THE UC3886 PWM CONTROLLER USES AVERAGE CURRENT MODE CONTROL TO MEET THE TRANSIENT REGULATION PERFORMANCE OF HIGH END PROCESSORS

by Larry Spaziani
Applications Engineer

ABSTRACT

The continuing development of high performance processors is imposing stringent requirements on their respective power systems. Intel's Pentium®Pro power system specification, for instance, demonstrates the industry trend to operate at lower voltages and at higher currents, with tight regulation and fast transient response. To meet these requirements, the UC3886 Average Current Mode PWM Controller is introduced. This application note highlights the features of the UC3886 and details how this IC is ideal for creating the optimal switching regulator for low voltage processor applications.

UC3886 FEATURES AND BENEFITS

- Average Current Mode Control direct from a sense resistor
  - No slope compensation networks required
- High Gain-Bandwidth Amplifiers for a fast transient response
- Programmable Current Sense Amplifier
  - Interfaces to a low power sense resistor
  - Accurate Over Current Protection
- On-board Reference for Standalone operation
- Direct Drive for Buck regulator NMOS high side switch
  - Eliminates need for separate Driver IC

INTRODUCTION

The Intel Pentium®Pro microprocessor specifications underscore an ongoing trend in high end digital systems. Clock frequencies are increasing for improved throughput and the number of transistors is increasing as manufacturing technology improves. Power management both within the processor and power to the processor has been elevated to a significant architectural design consideration.

The consequence of these advances for the power system is requirements that strike fear in the most hardy power supply designers. Load current increases as the number of transistors and the clock frequency increase whereas operating voltage decreases to limit the power dissipation on the processor. Noise immunity decreases as well under these conditions resulting in much tighter regulation requirements. High efficiency must be maintained even though currents are increasing and output voltages are decreasing. Load current transients become exceedingly fast as the processor goes into and out of sleep modes of operation. Operating voltage is no longer a standard but must be programmable for variations from supplier to supplier, or even within a product line, such as with the Intel Pentium®Pro. Of course, simplicity must be maintained in order to keep parts count low and cost down.

The UC3886 Average Current Mode PWM Controller has been created to meet these requirements. The UC3886 is a full featured PWM controller which offers excellent performance, yet can be configured as a basic Buck regulator with a low external parts count. Excellent regulation accuracy can be realized through the high gain of Average Current Mode Control and by the very low offset voltage and current amplifiers used in the UC3886, which contribute negligible error to the output voltage. High efficiency is maintained by providing a direct drive to an efficient, low $R_{DS(ON)}$ N-MOSFET. A variable output voltage power supply can be controlled simply by supplying a command voltage to the UC3886 from a programmable reference, such as the UC3910 4-Bit DAC and Voltage Monitor IC.

The high gain of Average Current Mode control offers several advantages which help the designer to meet the regulation requirements of a widely varying load current as well as the extremely fast transient requirements. High current loop gain can be maintained at low operating currents with a regulator in continuous or discontinuous modes of operation. Average Current Mode control also allows optimal high bandwidth loop compensation which can maintain regulation during high current transients. The UC3886 obtains this current information from a low value resistor, and requires no transformers or slope compensation circuitry. The highly accurate current limiting of the UC3886 reduces the need to electrically and thermally overdesign the power components for short circuit fault considerations.

THE UC3886 AVERAGE CURRENT MODE PWM CONTROLLER IC

A block diagram of the UC3886 is shown in Figure 1.

The UC3886 Average Current Mode PWM Controller is ideally suited for a basic Buck regulator configuration, as shown in Figure 2, where a low processor voltage is generated from +5V typically. Appendix 1 provides a review of the operation of the typical Buck regulator shown in Figure 2.

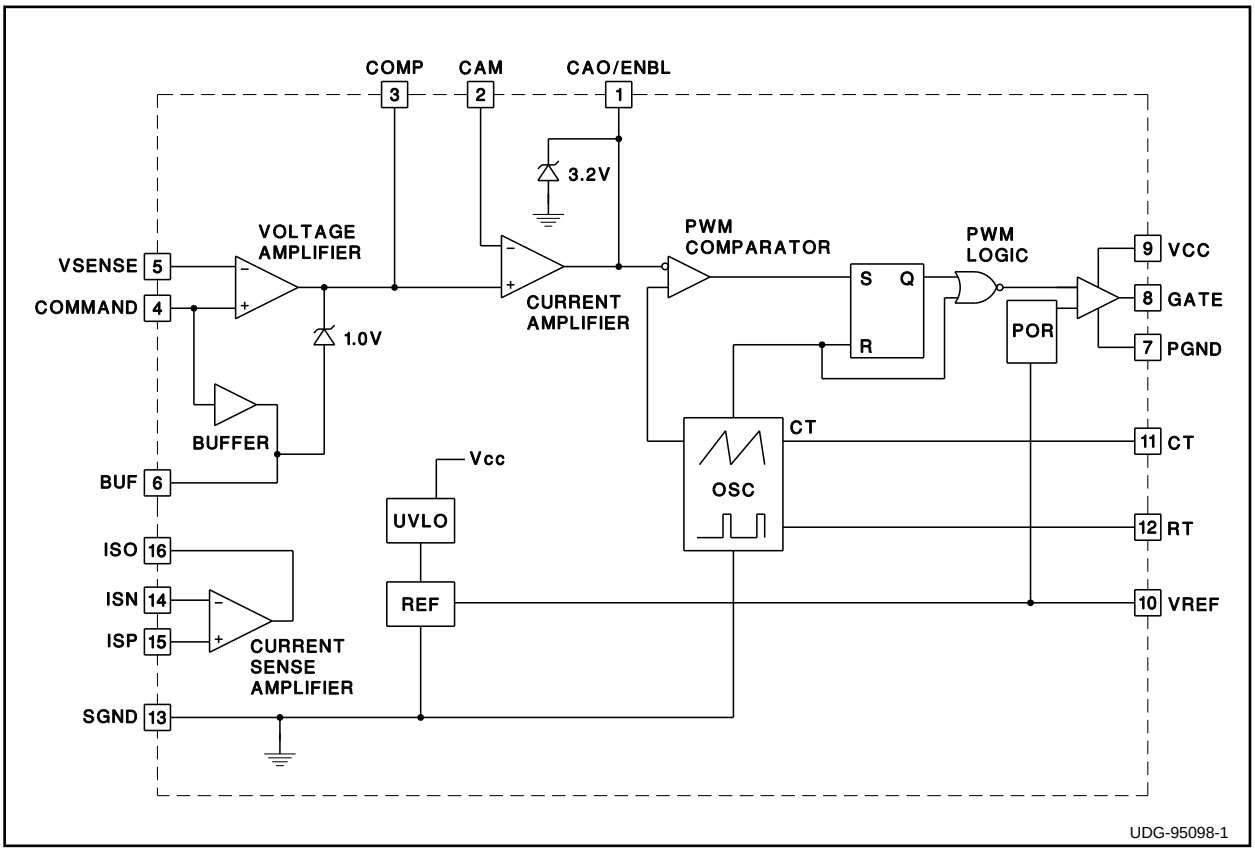

Figure 1. UC3886 Average Current Mode PWM Controller

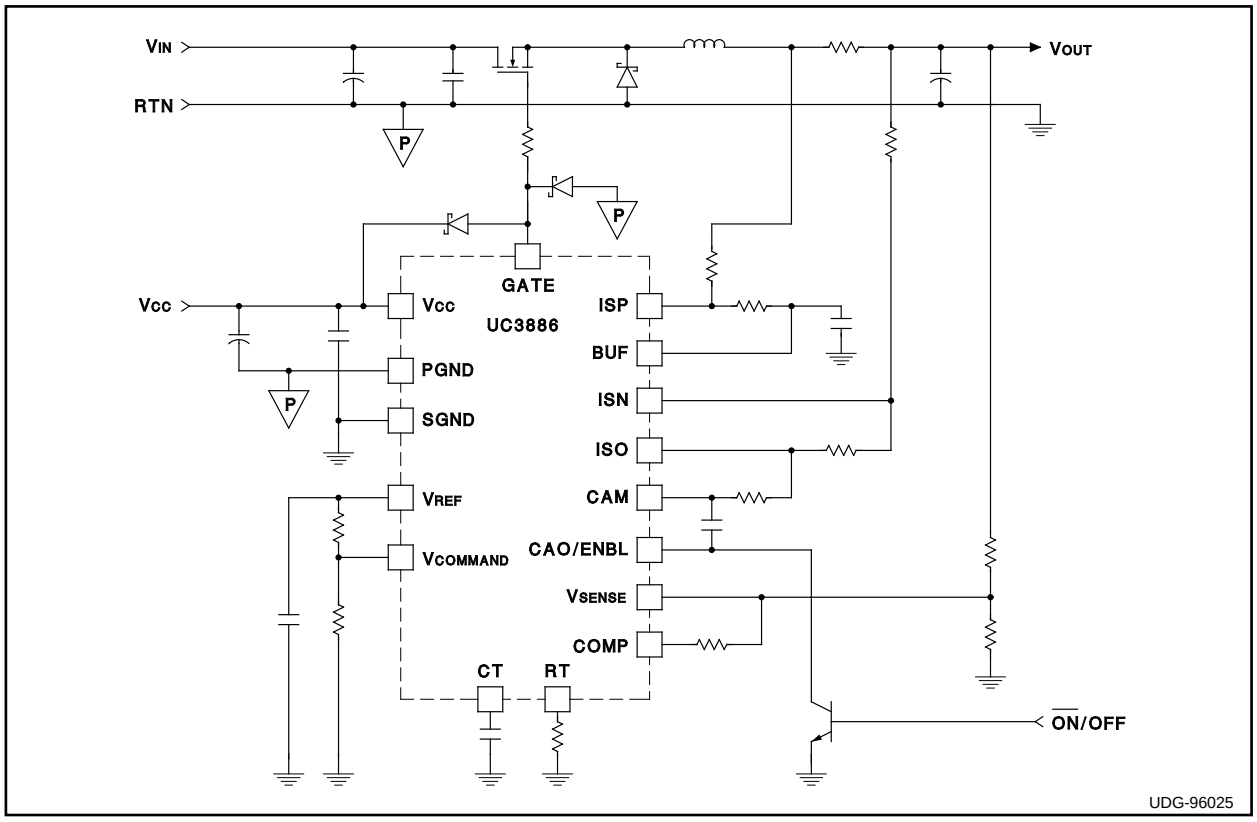

Figure 2. UC3886 Configured in a Typical Buck Regulator

UC3886 - SUPPLYING POWER

The UC3886 is constructed using a bipolar process allowing V_{CC} to be as high as 20V, however, the circuitry is optimized for a supply voltage of 12V. Minimum operating voltage is 10.3 volts. The supply voltage provides power directly to the reference voltage and the Gate Drive circuitry. It is also used to create an internal 7.3V bias voltage that supplies power to the Buffer, Voltage Amplifier, Current Amplifier, Current Sense Amplifier and the PWM comparator. The reference voltage is used to provide power directly to the PWM logic and to the Oscillator. Figure 3 shows the power distribution scheme within the UC3886.

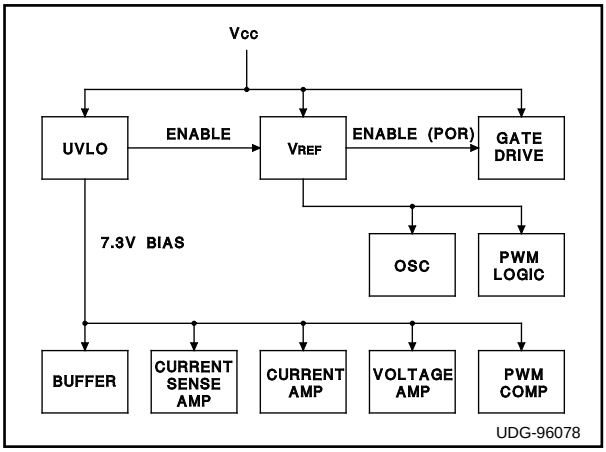

Figure 3. - Power Distribution within the UC3886

VCC should be decoupled to PGND closely to the IC with a low ESR capacitor to provide holdup during the gate pulses. Also add a 0.01µF to 0.1µF monolithic ceramic capacitor from VCC to SGND to provide high frequency signal decoupling.

UNDERVOLTAGE LOCKOUT

The UC3886 features an undervoltage lockout protection circuit for controlled operation during power up and power down sequences. Figure 4 shows typical V_{CC} thresholds of the UC3886 UVLO circuitry.

During UVLO, V_{REF} is kept off, which disables the oscillator, the PWM logic, and the Gate Drive. The

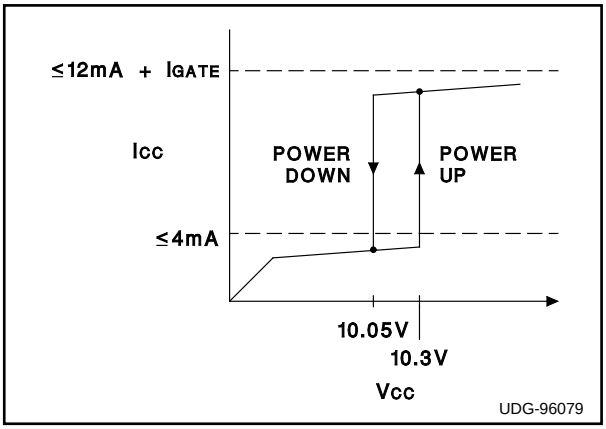

Figure 4. UC3886 UVLO Typical Values

buffers and amplifiers are also disabled. An internal signal called Power On Reset (POR) is created by monitoring the reference voltage, V_{REF}. The POR signal is held low until the reference voltage is high, at which time the Gate Drive output is enabled.

The total current drawn from the VCC source will include the IC supply current, I_{CC}, which provides bias power to the UC3886 as well as the average gate drive current, I_{GATE}, used to drive the N-channel MOSFET of the Buck regulator (see Appendix 2). The supply current is typically less than 4.0mA during UVLO and is typically less than 12mA (excluding gate drive current) when V_{CC} is above the UVLO thresholds. External loading of the reference voltage will add to the supply current, I_{CC}.

The 0.25V UVLO hysteresis prevents V_{CC} oscillations during the power up and power down sequences and also allows enough headroom for ripple voltage due to large gate drive current pulses.

Self Biasing, Active Low Output During UV Lockout

During UVLO, all chip functions are disabled in order to keep operating current at a minimum. The Gate Drive output, however, cannot be allowed to "float" high during this condition, because the Buck regulator N-channel MOSFET may inadvertently turn on.

An active low, self biasing totem-pole design is incorporated into the UC3886 Gate Drive output, which is very similar to that used in the UC3823A and is described in detail in U-128 [1]. The result of the self biased output is that during UVLO, the Gate Drive output is held low without drawing power from the supply voltage. No supply current is drawn because the self biasing output derives its power from the MOSFET gate voltage which is attempting to rise. This feature also negates the need for a gate-to-source resistor to keep the N-channel MOSFET biased off.

VREF

The UC3886 contains a 5.0V trimmed bandgap reference, similar to that used on many other Unitrode ICs. Figure 5 shows how the reference voltage, V_{REF}, can be used to create a Buck regulator command voltage ($V_{COMMAND}$) at the non-inverting input to the error amplifier, which sets the output voltage of the Buck regulator.

VREF can also be used to bias external circuitry, such as logic pull-ups and bias currents, so long as the total load current does not exceed 2.0mA. Short circuit protection on VREF protects the IC at a minimum of 10mA. A 0.01µF to 0.1µF monlithic ceramic decoupling capacitor from VREF to SGND should be located close to the IC.

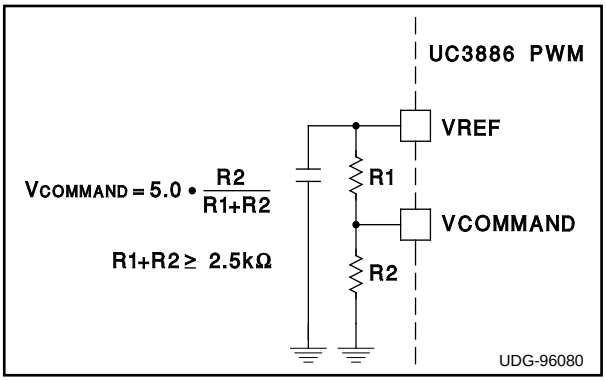

Figure 5. Setting VCOMMAND using VREF

HIGH POWER GATE DRIVE OUTPUT

The UC3886 features a single totem-pole output capable of directly driving an N-channel MOSFET and is similar to that of the UC3823A PWM IC. It features a 1.5A peak, 200mA average drive stage, ample capability to drive a size 6 FET [2] at several hundred kiloHertz.

The circuit of Figure 6 illustrates how the UC3886 Gate signal is used to drive a MOSFET for a low output voltage BUCK regulator.

Grounding with PGND and SGND

The PGND pin is a dedicated ground pin for the UC3886 output drive stage. The UC3886 Gate signal provides the high current gate pulses required during the MOSFET turn-on and turn-off times. These high current pulses should be decoupled by a low ESR capacitor placed closely to the IC as shown in Figure 6.

The current path for the gate pulses originates from the decoupling capacitor, passes through the totem-pole output of the UC3886 and enters the MOSFET gate. In a Buck regulator configuration, the inductor blocks the gate drive current, and therefore the gate current pulses exit the MOSFET DRAIN. The input capacitors decouple the gate current to ground and back to the V_{CC} decoupling capacitor, completing the loop. The PGND pin should be connected with the shortest possible path to power stage ground, to minimize loop inductance.

The SGND pin of the UC3886 is the reference voltage for all internal circuitry other than the output stage. SGND should have a direct path to the circuit ground, as shown in Figure 6, and should NOT be grounded at the PWM to PGND, since the gate pulses will result in some dv/dt in the PGND path. Differential voltage between SGND and PGND should not exceed 50mV.

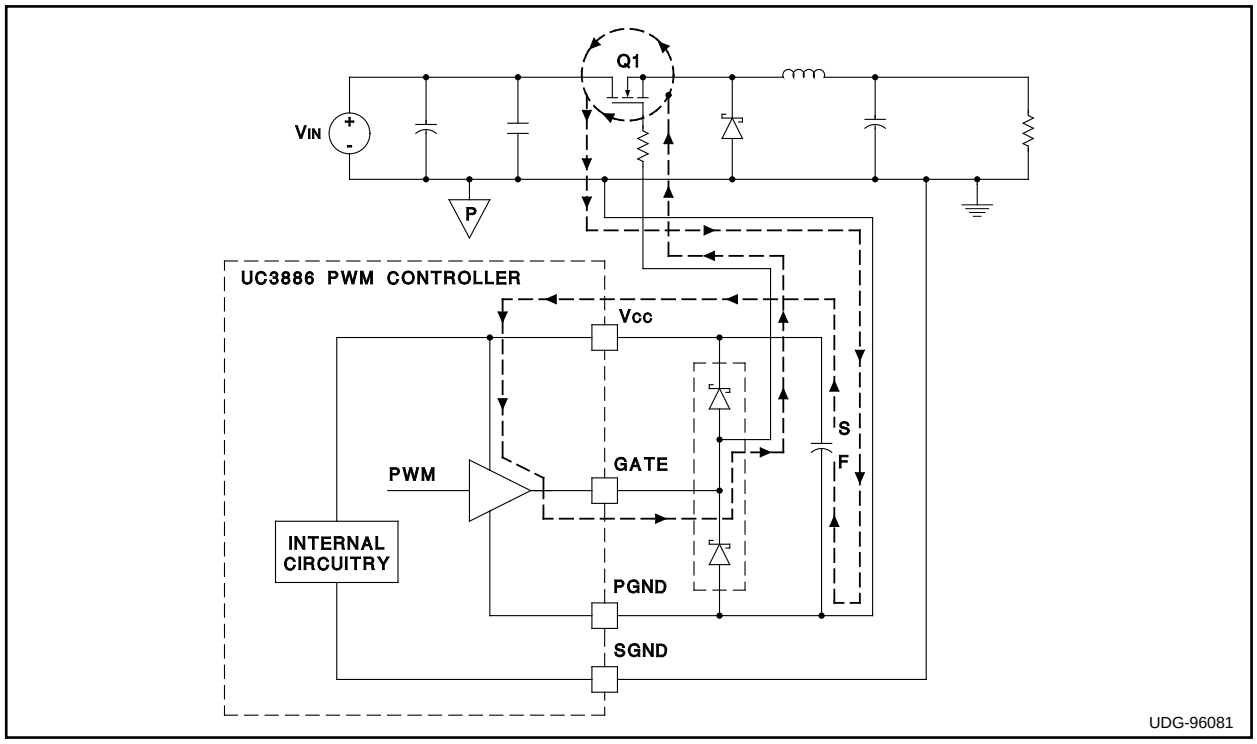

Figure 6. Driving a BUCK MOSFET with the UC3886

Schottky Clamping Diodes

The high di/dt characteristics of the gate drive pulse can cause undesirable ringing in the gate circuit, due to circuit trace inductance. A detailed explanation of why this occurs is available in Unitrode Application Note U-111 [2].

The use of low voltage schottky clamps, as shown in Figure 6, will protect the circuit from these effects. Use of 1N5821, 3A schottky diodes is recommended. The UC3612 is a dual schottky diode made specifically for this purpose and is available in an 8-pin DIP or SOIC package.

OSCILLATOR

The UC3886 oscillator is a sawtooth oscillator that is externally programmable (R_T, C_T) as shown in Figure 7. The oscillator switching period, T_S, consists of a charge time, T_C, and a discharge time or deadtime, T_D, such that

$$T_S = T_C + T_D \text{ [seconds]}$$

as shown in sawtooth waveform of Figure 7.

Oscillator equations presented below use the following units:

Resistance in ohms
Capacitance in farads
Currents in amperes
Time in seconds
Frequency in Hertz

The oscillator switching frequency, F_S, is given by

$$F_S = \frac{1}{T_S}$$

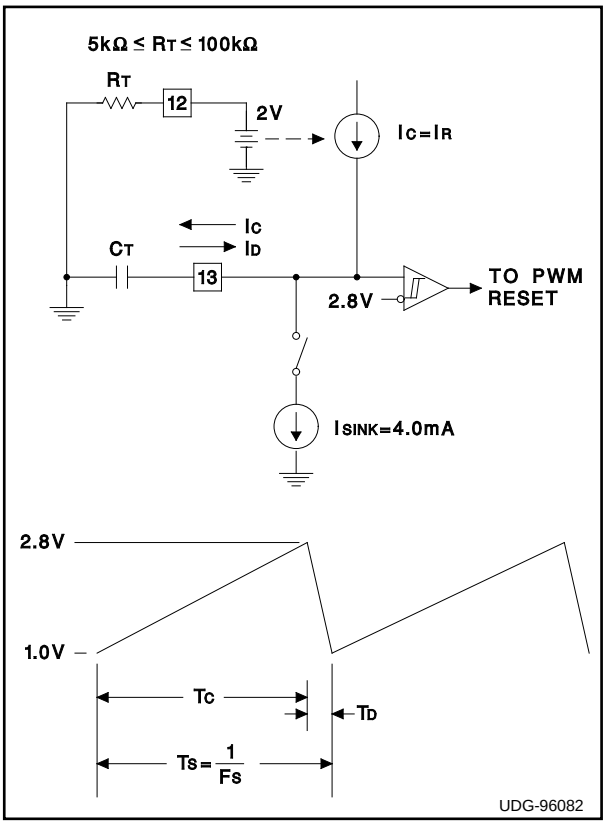

Figure 7. UC3886 Oscillator and Waveform

The sawtooth waveform charging current is programmed by the value of R_T. R_T should be a minimum of 5kW and a maximum of 100kW. Values of R_T outside this range will result in nonlinearity and are not recommended. The charge time is defined as the amount of time it takes the charge current to linearly charge C_T from 1.0V to 2.8V (DV = 1.8V), and is given by

$$T_C = \frac{C_T \bullet 1.8V}{(2.0V/R_T)}$$

The charge current is not switched off at the end of the charge time. The discharge current is therefore equal to

$$I_D = I_{SINK} - I_C = I_{SINK} - \frac{2.0V}{R_T}$$

where I_{SINK} is set internally in the UC3886 to 4.0mA.

The dead time is determined by

$$T_D = \frac{C_T \bullet 1.8V}{4.0mA - (2.0V/R_T)}$$

Programming the Oscillator

The first step in programming the oscillator is to choose a maximum operating duty cycle, D_{MAX}, given by

$$D_{MAX} = \frac{T_C}{T_C + T_D} = 1 - \frac{2.0V}{(R_T \bullet 4.0mA)}$$

D_{MAX} is programmable from 90% to 100%. Although a typical Buck regulator may only operate at 60% to 70% in steady state conditions, during a large transient load step condition, a higher duty cycle is required to “build” the inductor current. Programming D_{MAX} below 90% is not recommended. Figure 8 shows Dmax as a function of the timing resistor, R_T.

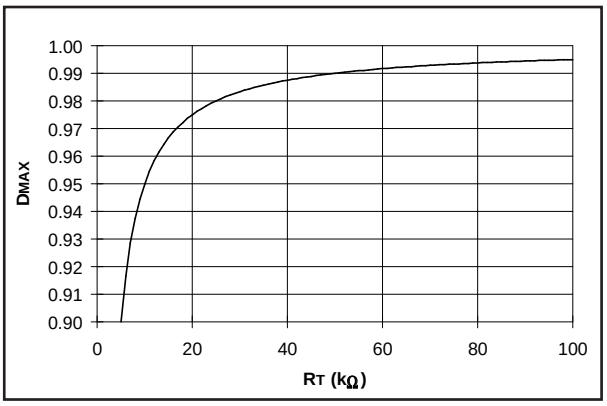

Figure 8. Programming Maximum Duty Cycle with R_T

The oscillator (switching) frequency can be programmed once the value of R_T is determined. The oscillator frequency is given by

$$F_S = \frac{2.0V \bullet [(4.0mA \bullet R_T) - 2.0V]}{C_T \bullet 1.8V \bullet R_T^2 \bullet 4.0mA}$$

which is plotted for several standard capacitor values in Figure 9.

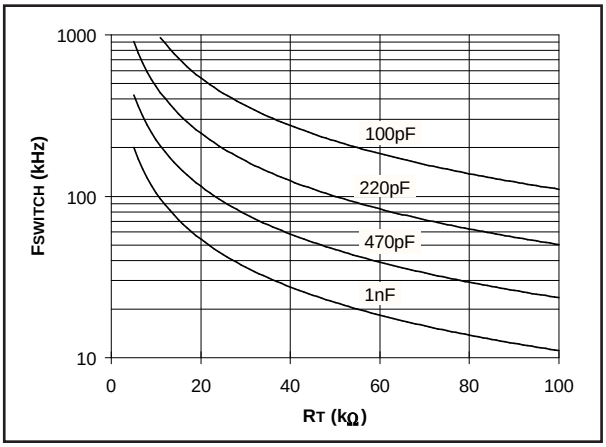

Figure 9. Programming Switching Frequency with C_T

Programming the oscillator frequency above 300kHz should be made with consideration for the Average Current Mode control amplifiers of the UC3886, which have an optimal Gain-Bandwidth product for operation below 300kHz.

The deadtime is plotted in Figure 10 as a function of R_T and C_T.

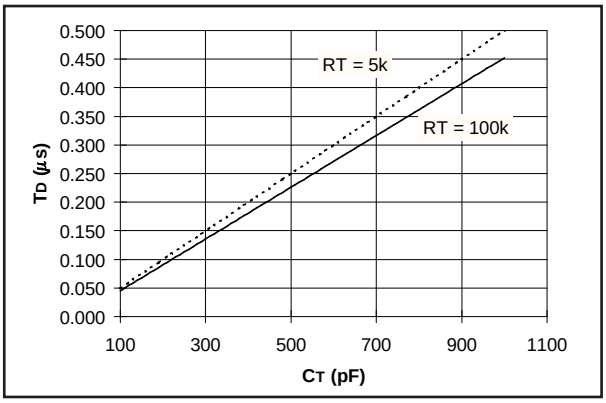

Figure 10. Deadtime vs C_T, R_T

Synchronizing the UC3886

Synchronizing the UC3886 can be achieved by superimposing a narrow voltage pulse on the PWM Ramp signal, as shown in Figure 11. The UC3886 oscillator should be programmed to freerun approximately 15% lower than that of the synchronizing frequency. A 1.0V amplitude pulse with a rise time of £ 10ns and a duration between 10ns and $T_D/2$ is recommended. Note that when synchronized, the dead time is the sum of the synchronizing pulse width and the oscillator discharge time. An excessively wide synchronizing pulse will result in less usable duty cycle, which may be required for large signal response. A very slow rising edge on the syn-

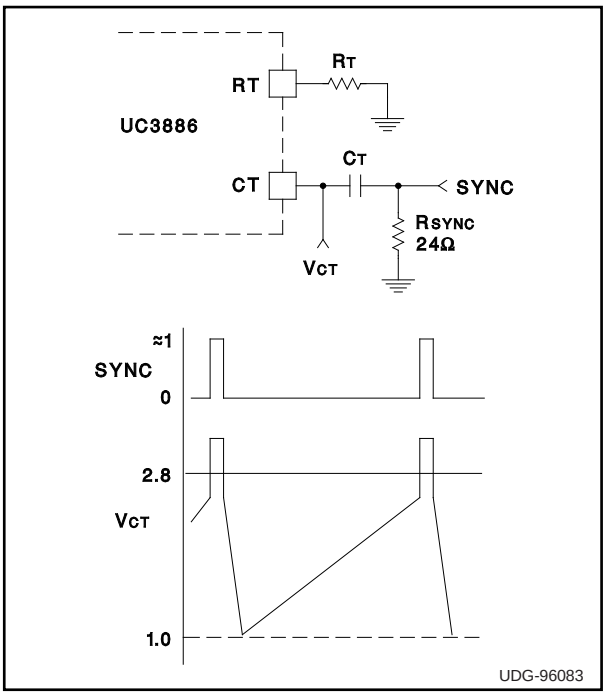

Figure 11. Synchronizing the UC3886

chronizing pulse should be avoided as well, as the PWM gain may be reduced.

Details of PWM oscillator operation, waveforms and synchronization is covered extensively in U-111 [2]. Synchronizing multiple UC3886 PWM controllers can be implemented using the UC3803 circuit as detailed in U-133A [3].

UC3886 - AVERAGE CURRENT MODE CIRCUIT BLOCK DESCRIPTION

The UC3886 Average Current Mode circuit blocks consist of the Voltage Amplifier, Buffer, Current Sense Amplifier, Current Amplifier and PWM Comparator. These blocks are shown in Figure 12 configured for Average Current Mode control in a Buck regulator.

The Dynamics of Average Current Mode Control with the UC3886

An understanding of the dynamics of Average Current Mode control as shown in Figure 12 is necessary to better understand the individual blocks which make up the system.

A simple but important fact must be understood up front; the ***load*** current of the Buck regulator is not the same as the ***inductor*** current of the Buck regulator. The ***load*** current is made up of the ***inductor*** current plus the current from the output capacitance. Average current mode control programs the ***inductor*** current. This is especially important when considering transient behavior and the dynamics involved.

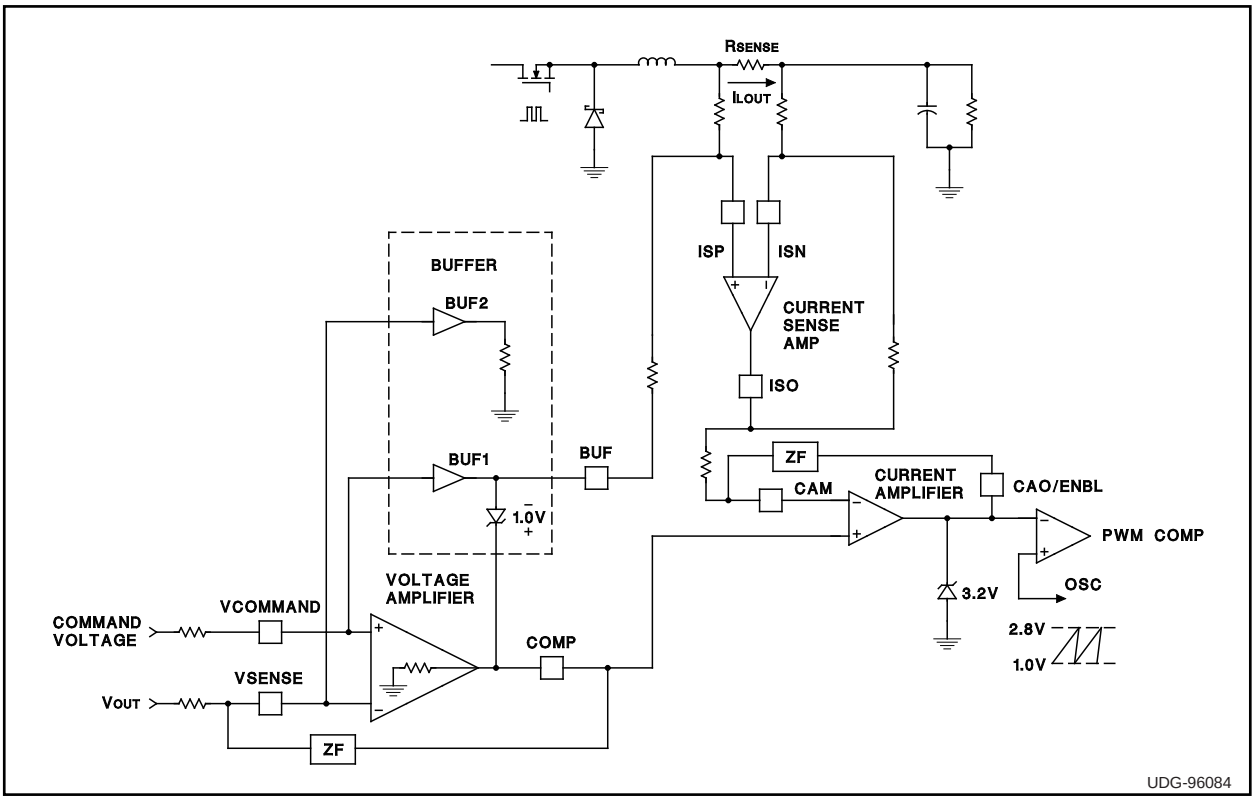

Figure 12. Configuring the UC3886 in Average Current Mode Control

The purpose of Average Current Mode Control is to program the Buck regulator (output inductor) to supply an average current to the load, such that the proper output voltage is maintained. The proper output voltage is programmed by the VCOMMAND pin on the UC3886.

A change in the load current of the Buck regulator will change the output voltage incrementally, which in turn will change the output of the Voltage Amplifier, COMP. Changing COMP will change the output of the Current Amplifier, CAO/ENBL, which is a direct input to the PWM comparator. Duty cycle will change as a result of CAO/ENBL changing. Note that at this point, the average inductor current has not changed yet, only the LOAD current. This means that until this point, the output capacitor has supplied the change in load current.

A duty cycle change will cause the average current to change through the inductor. The inductor current is converted to a voltage signal by the sense resistor, and is then amplified by the Current Sense Amplifier and is seen at the inverting input of the Current Amplifier, CAM. When the amplified current signal of the Current Amplifier's non-inverting input is equal to the COMP pin, the circuit settles into a steady state condition, where the average current into the load results in the proper output voltage.

BUFFER

The UC3886 Buffer block performs three functions:

- Buffers VCOMMAND to create a bias voltage for the Current Sense Amplifier output ISO.
- Clamps the COMP output of the Voltage Amplifier to:

  1.0 volt above the command voltage for use in current limiting.

  0.7 volts below the command voltage to limit large signal swing.
- Buffers V_{SENSE} for the sole purpose of minimizing the offset voltage at the Voltage Amplifier (BUF2 in Figure 12).

The Buffer has a gain accuracy of 1.0 ±0.05 V/V. A decoupling capacitor of 0.1µF located close to the IC is recommended in order to reduce noise in the current loop and to insure the unity gain stability of the Buffer.

VOLTAGE AMPLIFIER

The UC3886 Voltage Amplifier is used to create an error voltage based on the difference between the non-inverting (VCOMMAND) and inverting (VSENSE) inputs to the Voltage Amplifier. It features a 3.5MHz Gain-Bandwidth product and an open loop gain of 85dB.

The Voltage Amplifier is optimized to provide excellent DC accuracy in a closed loop system by providing low offset voltage (±2.0mV) and very low input offset current (±0.01uA). The second buffer, BUF2, which buffers the VSENSE line, also improves DC accuracy by insuring that its bias current is closely matched to the bias current of BUF1 (i.e., very low offset current between BUF1 and BUF2). By matching the impedances at the Voltage Amplifier inputs, as shown in Figure 13, the low Voltage Amplifier and Buffer bias currents will cancel, minimizing DC error. Reducing the values of the resistors will minimize this small offset error.

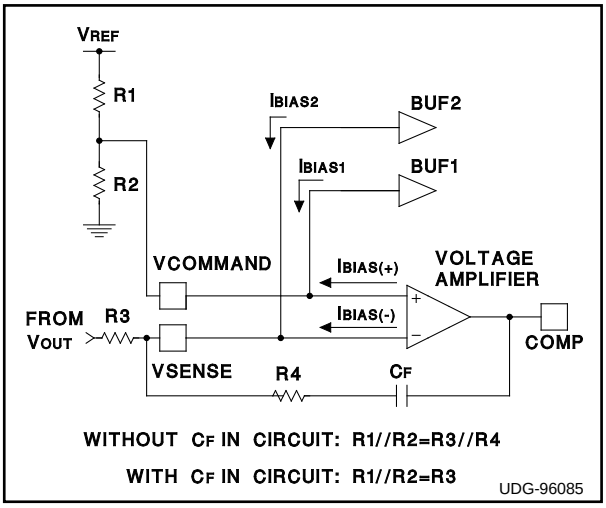

Figure 13. Minimizing DC Offsets at the Voltage Amplifier

The Voltage Amplifier is also optimized for large signal transient performance. A large signal (step) load change in a Buck regulator will result in a rapidly changing output voltage, which in turn will cause the Voltage Amplifier's output (COMP) to change. The COMP pin is clamped by the buffer to V_{BUF} +1.0V on the high side and to V_{BUF} -0.7V on the low side, where V_{BUF} is the voltage at the BUF pin. This insures that large signal transitions at the COMP pin will be limited to just outside its steady state control range (V_{BUF} to V_{BUF} +1.0V). Feedback capacitors will not have to be charged up and discharged from "rail to rail", and therefore the Voltage Amplifier will react much more quickly to transients, reducing reaction time and overshoot. Using low feedback capacitance will allow the Voltage Amplifier to rapidly slew from one level to another, insuring excellent transient response.

The use of non-integrating feedback around the Voltage Amplifier can optimize the transient performance of a converter by minimizing the amount of

capacitance on the COMP pin, and by intentionally limiting DC voltage regulation. Non-integrating compensation is discussed in Appendix 3.

CURRENT SENSE AMPLIFIER

The UC3886 Current Sense Amplifier is used to amplify a differential current sense signal across a low value current sense resistor, R_{SENSE}. It features a 2.5MHz Gain-Bandwidth product and an open loop gain of 85dB. This amplifier must be set up as a differential amplifier as shown in Figure 14. A differential amplifier configuration will amplify only the difference voltage across the sense resistor, R_{SENSE}, and will not amplify or carry common-mode information.

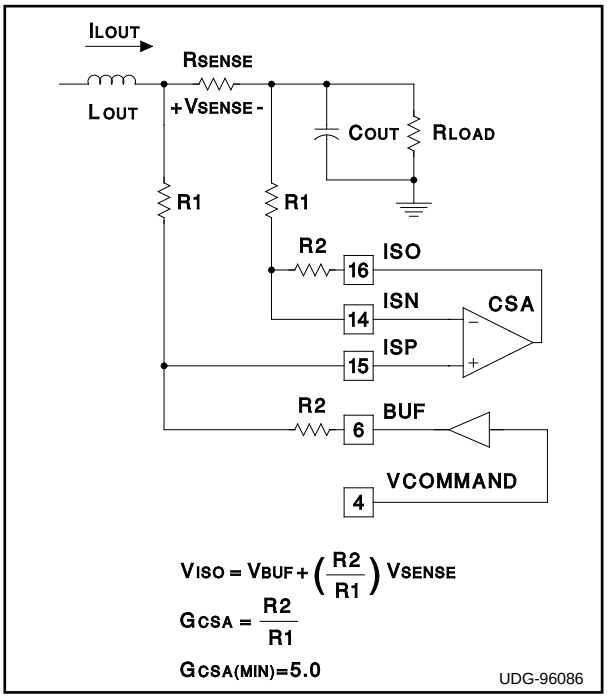

Figure 14 . Configuring the Current Sense Amplifier of the UC3886

The Current Sense Amplifier gain must be programmed (by external resistors) to be greater than or equal to 5.0 (14dB), as this amplifier ***is not stable*** with gain below 5.0. The Current Sense Amplifier gain is limited on the high side by its Gain-Bandwidth product of 2.5MHz. Therefore, the gain of the Current Sense Amplifier, G_{CSA}, must be programmed between

$$G_{CSA\_MIN} = 5.0 \text{ and } G_{CSA\_MAX} = 2.5MHz/F_{SWITCH}$$

where F_{SWITCH} is the oscillator switching frequency.

Equations governing a Differential Amplifier are contained in Appendix 4.

R_{SENSE}, the current sense resistor, is used to measure the output inductor current, which is necessary for the proper operation of Average Current Mode Control. The Current Sense Amplifier features a common mode input range from 0.0 to 4.5Vdc. This allows the current sense resistor to be placed directly in series after the output inductor in low output voltage converters.

R_{SENSE} should not be placed before the output inductor because the current sense signal will be outside the common mode range of the Current Sense Amplifier. Likewise, R_{SENSE} should not be placed in the return path unless a ground difference can exist between the UC3886 and the load, which may be detrimental to voltage regulation. Figure 15 illustrates these points.

CURRENT AMPLIFIER AND PWM COMPARATOR

The Current Amplifier is used to create a current error voltage based on the difference between the amplified inductor current and the Voltage Amplifier output, COMP. It features a 3.5MHz Gain-Bandwidth product and an open loop gain of 85dB. Using an integrating feedback compensating network around the Current Amplifier presents two advantages of Average Current Mode control over Peak Current Mode Control [4]. Higher DC gain is the first advantage. The second is the ability to compensate the loop, whereas Peak Current Mode Control has a fixed gain.

The output of the Current Amplifier, CAO/ENBL, is compared to the PWM ramp with the result being a duty cycle varying as a function of the inductor current and the commanded voltage. Ideal PWM comparator waveforms are shown in Figure 16. By observing the waveforms of Figure 16, the noise immunity advantage of Average Current Mode control over Peak Current Mode control can be seen. At the beginning of each switching cycle, the Ramp signal is at its lowest point, and therefore the PWM comparator is less susceptible to turn on spikes. Also, since an Average Current Mode control system samples the Inductor current, and not the switch current, there are no parasitic turn on spikes to compensate for or filter.

The Current Amplifier output, CAO/ENBL, is compared to the ramp waveform generated at the timing capacitor, C_T, at the high speed PWM Comparator. The ramp waveform is a fixed frequency ramp ranging from 1.0V to 2.8V. Figure 16 shows that the output of the Current Amplifier is clamped to approximately 3.2V, which is above the steady state range of the PWM comparator (2.8V). Large signal transient conditions may cause the Current Amplifier output to swing high and clamp to this upper limit. Clamping the Current Amplifier output allows a fast transient response, as the feedback

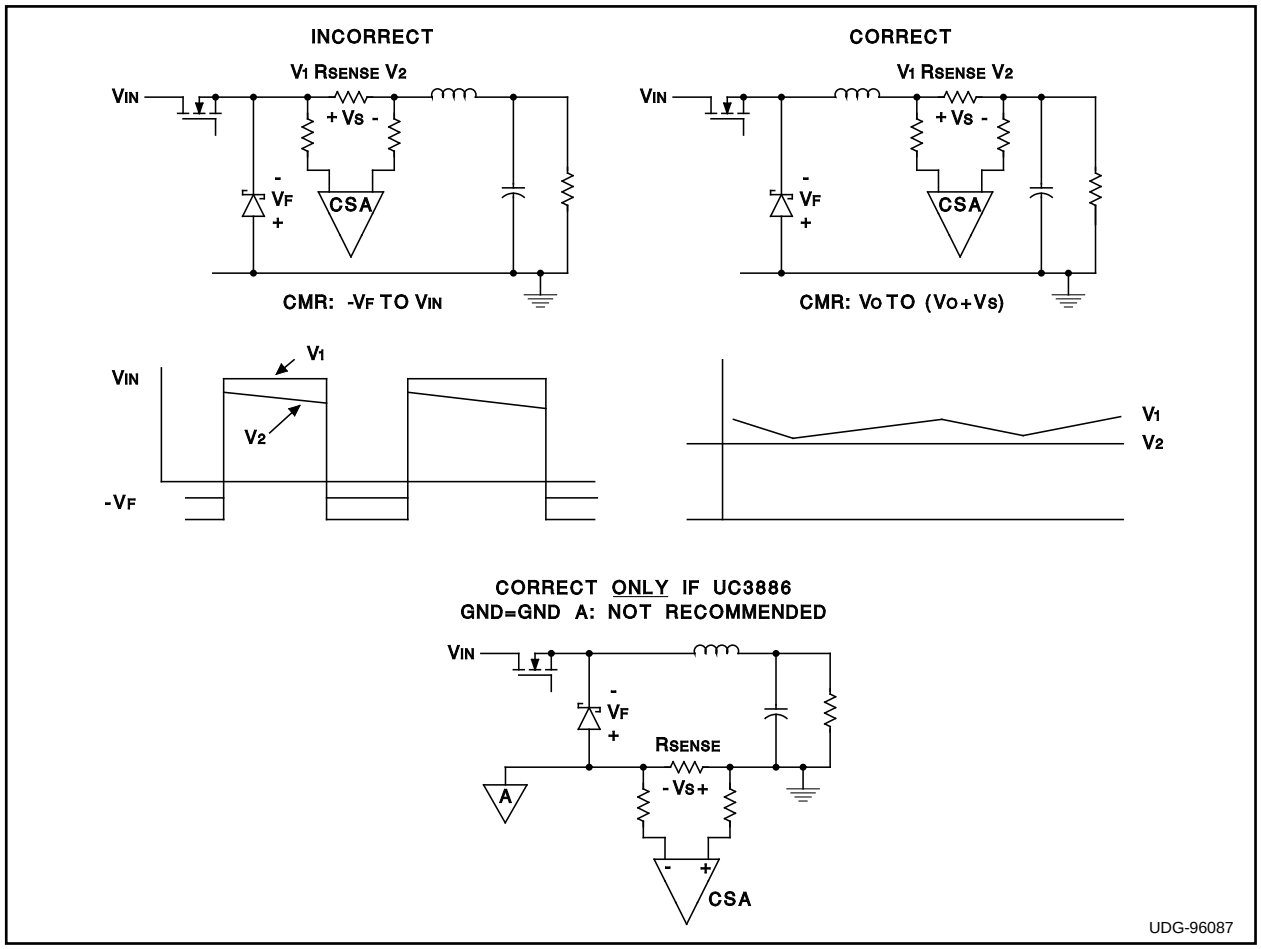

Figure 15. Sense Current AFTER the Inductor to Insure the Signal is within the Current Sense Amplifier's Common Mode Range

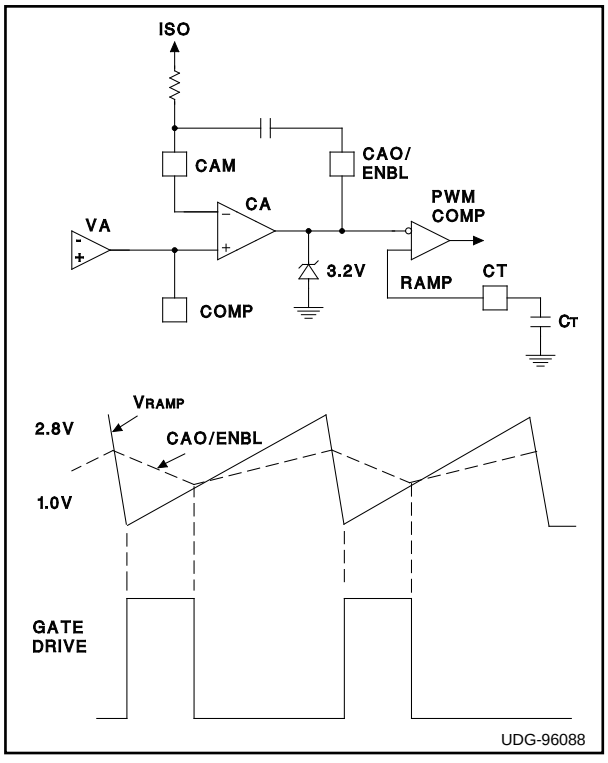

Figure 16. The Current Amplifier Output is compared to the PWM Ramp Signal

capacitors do not swing over a large voltage range and cause substantial transient overshoots or delays.

Disabling the UC3886 Gate Output with CAO/ENBL

The UC3886 can be disabled by bringing the CAO/ENBL pin below 0.8V, as shown in Figure 17. The CAO/ENBL pin is one input to the PWM comparator, and the oscillator ramp waveform is the other. Bringing the CAO/ENBL pin below 0.8V will force the Gate Drive duty cycle to 0%.

The CAO/ENBL is the output of the Current Amplifier and will be compensated for loop control. The signal to the CAO/ENBL pin must therefore be a true open collector so that during the HIGH (open) state, there is no effect on the amplifier's performance. The open collector signal must be capable of sinking ^{3} 250µA and remain below 0.8V. Figure 17 shows R1 which is recommended if the enable signal is located at a significant distance from the power supply. A long circuit board signal run can couple noise into the current loop if it resides close to noisy signals. R1 acts as a high impedance block to noise signals. R1 should be

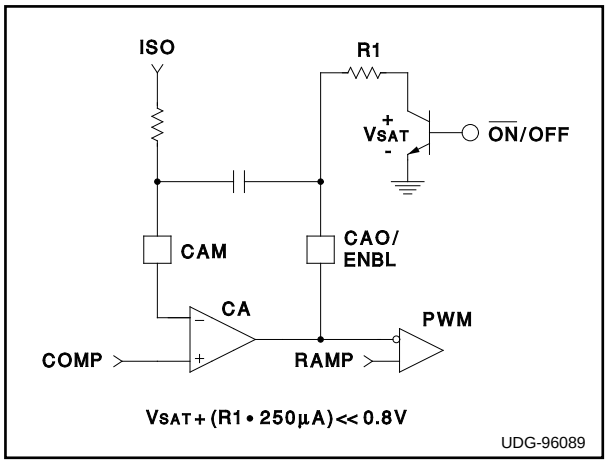

Figure 17. Disabling the UC3886

small enough however to insure that the disabling signal at CAO/ENBL is less than 0.8V. A 1kW resistor is recommended.

No features of the UC3886 are powered down during the disabled output state other than the Gate Drive output.

CLOSING THE LOOP WITH AVERAGE CURRENT MODE CONTROL

The fundamental principles of Average Current Mode Control are presented in Unitrode Application Note U-140 [4]. Compensating both the current loop and voltage loop is further detailed in Unitrode Seminar Topic “Switching Power Supply Control Loop Design” [5].

Figure 18 is a modification of the models presented in the two referenced application notes where the addition of the Current Sense Amplifier is the fundamental change.

Closing the Loop in a Variable Output Power Supply

The above mentioned references on closing the loop using Average Current Mode control show a critical limitation on the inductor current slope during the switch OFF time. A variable output power supply must consider the maximum operating output voltage, where the inductor current OFF time slope is maximized. The result will be less than optimal gain at the lower operating voltages.

CURRENT LIMITING WITH THE UC3886

The output of the Current Sense Amplifier, ISO, is determined by the differential gain equation (see Appendix 4) and is biased by the voltage at the BUF pin, V_{BUF}, as shown in Figure 14, such that

$$ISO = V_{BUF} + V_{SENSE} \bullet G_{CSA} \text{ [Volts]}$$

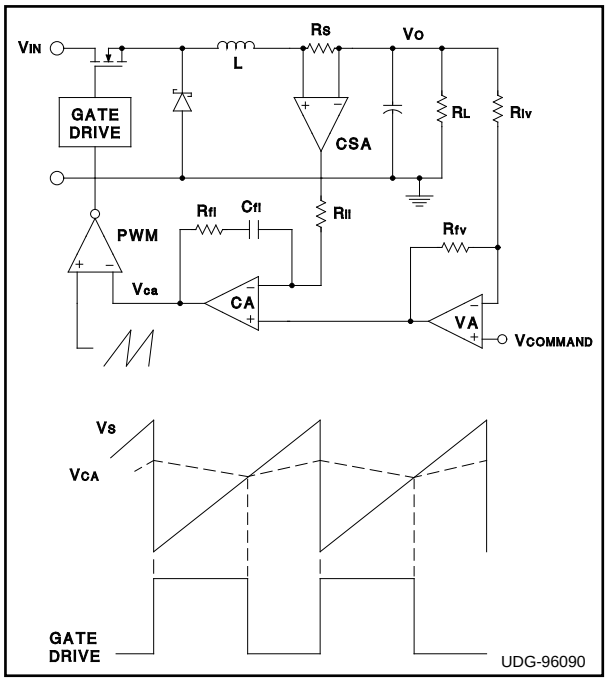

Figure 18. Average Current Mode Control Circuit and Waveforms for the UC3886 ACM Controller

where

$$V_{SENSE} = I_{LOUT} \bullet R_{SENSE} \text{ and}$$

$$G_{CSA} = \frac{R2}{R1} \text{ as shown in Figure 14.}$$

An increase in load current will force the power supply output voltage to decrease as the output capacitor discharges. This will force the Voltage Amplifier output (COMP) upward, the Current Amplifier output (CAO/ENBL) higher, will increase the duty cycle and thus will increase the inductor current.

COMP is clamped to V_{BUF} + 1.0V by the buffer. As the average output inductor current continues to rise, to raise the output voltage, the output of the Current Sense Amplifier, ISO, exceeds the value of COMP. This occurs when

$$I_{SC} \bullet R_{SENSE} \bullet G_{CSA} = 1.0 \text{ Volt}$$

or at a short circuit current limit, I_{SC}, of

$$I_{SC} = \frac{1.0 \text{ Volt}}{R_{SENSE} \bullet G_{CSA}} \text{ [Amperes]}$$

When ISO exceeds the value of COMP, the Current Amplifier, configured for high DC gain, swings to its minimum value, resulting in a lower short circuit duty cycle, D_{SC}. D_{SC} is high enough only to maintain the average current through the inductor.

Figure 19 graphically represents the dynamics of a short circuit placed across the output of the Buck regulator of Figure 12 at time t_1.

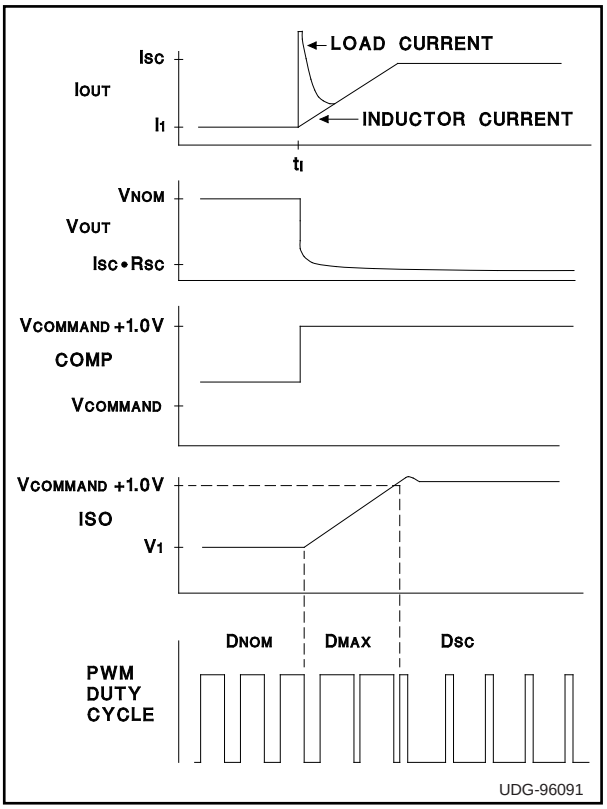

Figure 19. Dynamics of Short Circuit Protection with the UC3886

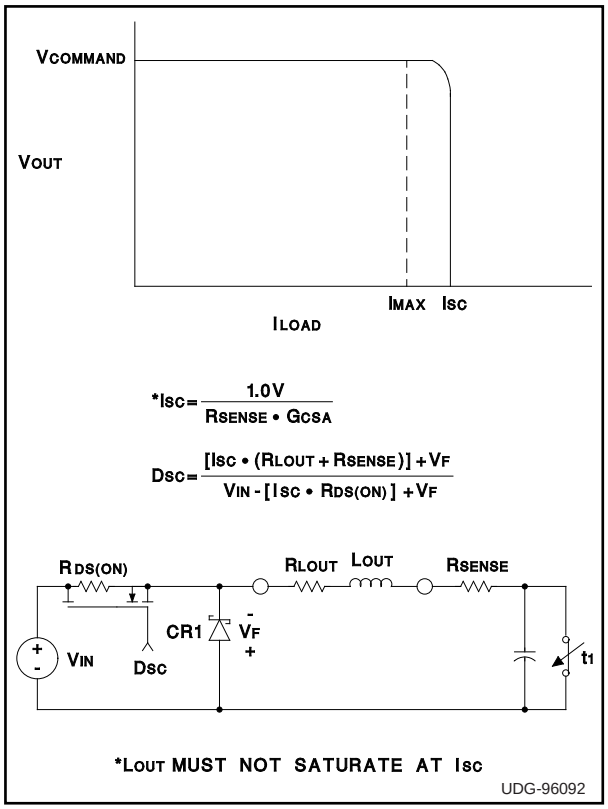

Figure 20. UC3886 Current Limit Load Line in a Buck Regulator

Current Limit Load Line

Current limiting in the UC3886 follows a “square knee” load line, where current is not disabled or folded back. Figure 20 shows this load line.

The voltage at the output of the Buck regulator of Figure 20 falls proportionally to the value of the short circuit, usually measured in milliohms. Many regulators, under a short circuit of extremely low resistance, will demonstrate a condition where Ipeak can be much larger than I_{SC}, often referred to as “tail-out”. Safety and reliability issues may arise should the value of Ipeak not be well understood and controlled.

The simplified Buck regulator shown in Figure 20 shows several key parasitic elements, along with the value of R_{SENSE}, which limit the current to I_{SC}, preventing tail-out. See Appendix 5 for a detailed example of programming the current limit using the UC3886 ACM Controller.

AVERAGE CURRENT MODE CONTROL IN DISCONTINUOUS MODE

Average current mode control offers the advantage of being able to function while the regulator is running in a discontinuous mode of operation where the output inductor, and therefore the current signal, runs dry.

With peak current mode control, during discontinuous mode, the peak/average current error becomes unacceptably large, a result of the fixed and limited gain in peak current mode control. The high gain of the Current Amplifier used in Average Current Mode control allows the large changes in duty cycle required for load changes. The Average Current Mode gain, however, is limited.

There is a slope limitation criteria of Average Current Mode control (U-140 [4]) which is: *The amplified inductor current downslope at one input of the PWM comparator must not exceed the oscillator ramp slope at the other comparator input.* This slope criteria directly limits the amount of gain obtainable in the Current Amplifier at the switching frequency.

The criteria mentioned above can be equated as

$$\frac{V_O + V_F}{L_{OUT}} \bullet R_S \bullet G_{CSA} \bullet G_{CA} \pounds \frac{V_S}{T_S - T_D}$$

where, in the model of Figure 18

V_S = Oscillator Ramp [V]

T_S = Switching Period [s]

T_D = Oscillator Deadtime [s]

V_O = Output Voltage [V]

V_F = Freewheeling Diode Forward Voltage [V]

L_{OUT} = Output inductor [H]

R_S = Sense Resistor [W]

G_{CSA} = Gain of the Current Sense Amplifier

G_{CA} = Gain of the Current Amplifier at the switching Frequency.

It can be shown from the above equation that the Current Amplifier gain is directly proportional to the Inductor value, and is constant at a given output voltage.

$$\frac{G_{CA}}{L_{OUT}} = \frac{V_S}{T_S - T_D} \bullet \frac{1}{R_S \bullet G_{CSA}} \bullet \frac{1}{V_O + V_F} = K$$

Decreasing L_{OUT} must result in a decrease in G_{CA}, and therefore the Average Current Mode gain. This lower current gain will adversely effect large signal response of the circuit, although a smaller inductor value will improve large signal response. Even with this limitation on the gain G_{CA}, Average Current Mode Control can achieve much higher gains than Peak Current Mode control.

STARTUP AND SOFT STARTING WITH THE UC3886

Soft starting a power supply is defined as bringing the output voltage up to its specified value in a slow, controlled manner. Typical power supplies soft start in 10ms to 100ms.

The need for soft starting a power supply is often associated with overshoot. The output voltage of a power supply will often ring over its specified value when the power supply is “snapped” on, as the control loop often lags the rise of the output voltage. The overshoot can be destructive if it is not clamped or controlled. Slowly ramping up the output voltage will minimize the overshoot.

The fast transient response of the UC3886 Average Current Mode controller helps eliminate the need for soft starting the DC/DC converter. At startup, the Average Current Mode control directly controls the inductor current. As long as the output voltage is less than the required voltage, the current loop forces the UC3886 to supply current limited to I_{SC}, the short circuit limit. Once the proper output voltage is reached, the very fast transient response of the UC3886 Voltage and Current Amplifiers will cut back on the duty cycle, thus eliminating the voltage overshoot associated with a slow loop response. A large output capacitance on the DC/DC converter will insure that a slight overshoot in inductor current results in negligible overshoot in the output voltage.

A soft start capacitor can be added to the VCOMMAND pin as shown in the circuit of Figure 21, should a slow, controlled start up be required. The values or resistors R1 and R2 should be chosen to (a) create the proper voltage at VCOMMAND, (b) draw less than 2.0mA from VREF and (c) equal the impedance seen by the inverting input of the UC3886 Voltage Amplifier, V_{SENSE}, to cancel bias current effects. Once the resistors are chosen, then C_{SS} should be chosen for the proper time constant.

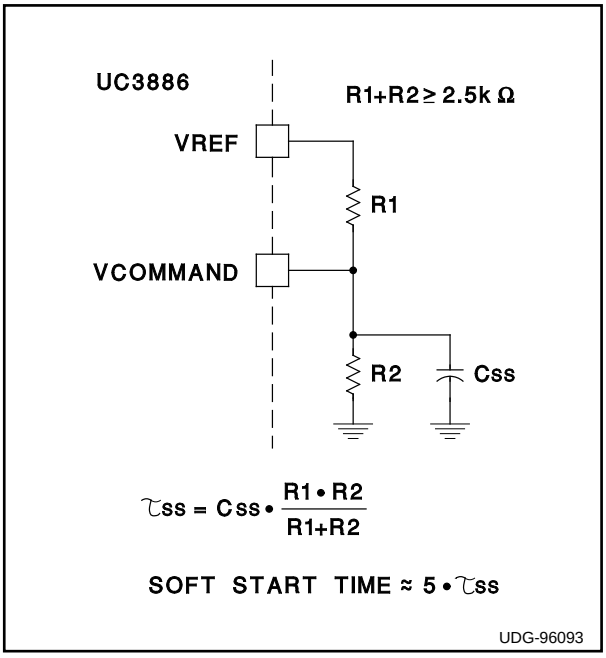

Figure 21. Soft Starting the UC3886

DRIVING A HIGH SIDE N-CHANNEL MOSFET WITH THE UC3886

The UC3886 is designed to drive an N-Channel MOSFET in a Buck configuration, as shown in Figure 6. There are circuit and MOSFET factors to be considered in order to properly drive the MOSFET. The circuit factors include the values of V_{IN}, V_{CC}, UVLO, the UC3886 totem-pole gate voltage and ringing voltages on the Gate and Source nodes. The MOSFET factors include V_{GSmin}, V_{GSmax}, R_{DSon} vs V_{GS}, and the type of MOSFET used, standard or Logic Level. A MOSFET’s on and off characteristics are controlled by the gate-to-source voltage, V_{GS}.

There are many sources of literature [6, 7, 8, 9] which discuss MOSFET drive circuits and parameters. This application note will highlight several considerations in using the UC3886 GATE output in dri-

ving standard and Logic Level MOSFETs in a Buck regulator.

Standard MOSFET

1) Given a 5 volt input and a 12 volt V_{CC} source to the UC3886 (Figure 6), V_{GS} is only 7 volts nominally. R_{DSon} for standard MOSFETs is often specified with V_{GS} = 10V. A survey of several 60 volt low R_{DSon} MOSFETs shows that R_{DSon} is higher by a factor of approximately 1.35 when these MOSFETs are driven with only 7 volts V_{GS}. Specific data sheets and curves should be reviewed for exact figures.

2) The UVLO threshold at startup for the UC3886 is 10.3 volts. Although the PWM will start switching when UVLO is disabled, there may not be enough gate-to-source voltage for the MOSFET to carry the full load current. This characteristic can effect the amount of time to reach full load current at startup.

3) Turn on time for standard MOSFETs is often specified with V_{GS} = 10V, whereas the initial gate-to-source voltage from the UC3886 may be less than 10V. The resulting turn on time may be longer than specified in the device data sheets.

Logic Level MOSFET

1) Many modern, low voltage, low R_{DSon} Logic Level MOSFETs have a maximum V_{GS} rating of ±10V. Excessive gate voltage may damage or seriously degrade the reliability of these MOSFETs.

In the Buck regulator of Figure 6, the source voltage is rising from $-V_F$ to $+V_{IN}$ during turn on. At the beginning of the cycle, the gate-to-source voltage, V_{GS}, is equal to $V_{GATE}+V_F$, which may be well in excess of 10V. At the end of the cycle, V_{GS} is less, as the source voltage has risen to approximately the input voltage. The gate-to-source voltage dynamic characteristics are dependent on the value of series gate resistance, R_{GATE}, as well as circuit load characteristics. R_{GATE} can be increased to insure that during the turn-on pulse, the source voltage has risen to the input voltage well in advance of V_{GS} reaching its maximum value. The cost of this approach may be in switching power losses.

A gate-to-source zener diode can be used as shown in Figure 22 to insure that excessive V_{GS} is not reached.

Low R_{DSon} - Low Voltage MOSFETs

Several MOSFET processes have increased the density of MOSFET cells in order to optimize R_{DSon} and current handling capabilities. One result of this is the reduction of a good Gate metal path to individual cells. The result of this is higher internal gate resistance and inductance, which effects the switching performance of the MOSFET.

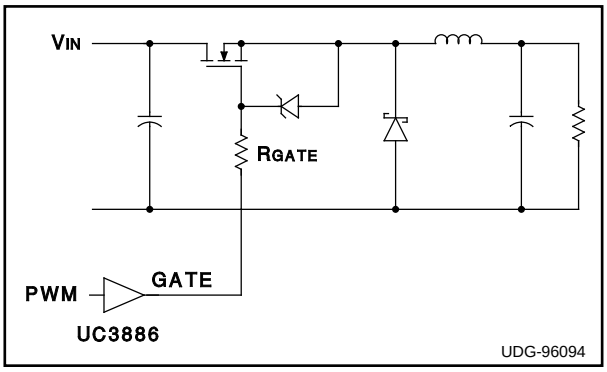

Figure 22. Clamping V_{GS} with a Zener Diode

A noticeable effect of these parasitics is the difference between the Turn-On delay and the Turn-Off delay. At turn-on, as soon as a small number of cells are turned on, drain current begins to conduct. At turn-off however, the gate charge must be removed from all MOSFET cells, resulting in a substantial delay in turning off the drain current, as illustrated in Figure 23. MOSFET Turn-on and Turn-off delays will vary based on supplier processes. Supplier data sheets should be consulted.

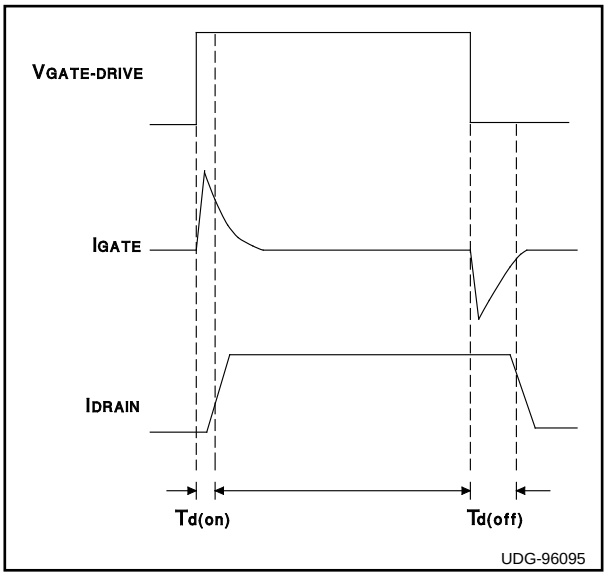

Figure 23. MOSFET Turn-On and Turn-Off Delays

USING THE UC3886 WITH THE UC3910 FOR A COMPLETE Pentium®Pro SOLUTION

The UC3886/UC3910 Chip Pair is shown in Figure 24 as configured in a typical Buck regulator. The programmable DAC output of the UC3910 is simply fed into the VCOMMAND pin of the UC3886 to provide a programmable PWM controlled power supply.

Using this chip pair offers significant benefits when providing power to today's microprocessors. The two IC's can be configured, as shown in Figure 24, to provide all functions required to interface with,

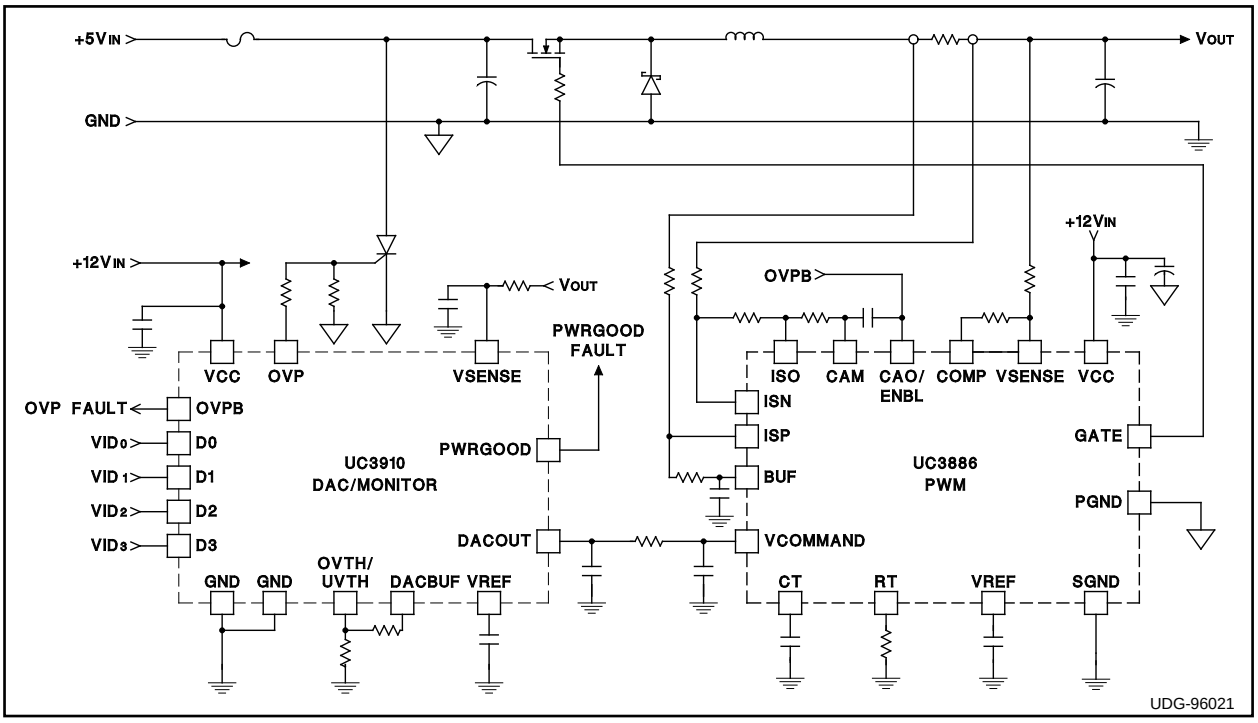

Figure 24. UC3886/UC3910 Interconnection Diagram

control, and monitor the performance of the Intel Pentium®Pro and other high end processors. Together, the chip pair meets the critical requirements of the Pentium®Pro with a simple, accurate and efficient switching regulator which meets the difficult transient regulation requirements with Average Current Mode Control.

For additional information on the UC3910 4-BIT DAC and Voltage Monitor IC, refer to application note U-158 [10]. For additional information on a detailed circuit design and performance of the UC3886/UC3910 chip pair, refer to application note U-157 [11].

Features of the UC3886/UC3910 Chip Pair

Simplicity

The UC3886/UC3910 is configured to drive a basic Buck regulator. The ICs integrate all control and monitoring functions, so that external parts count is reduced. Circuit boards can use fewer layers, fewer interconnects and fewer components.

The UC3886 features a direct output NMOS drive, eliminating the need for creating high voltages and allowing the use of an efficient N-Channel MOSFET.

The programmable voltage feature of the UC3910 allows system designers to directly interface with Intel's Pentium®Pro to create one power supply that will meet all voltage requirements, and thus reducing all the logistics associated with single output power supplies.

The UC3910's DAC and unique voltage monitoring architecture directly replaces discrete components including a precision reference, a DAC, complicated resistive networks, multiple window comparators and an SCR Driver. The UC3910's tracking fault windows are simply programmable with two external resistors.

The UC3886 can directly monitor the inductor current through a low value resistor, eliminating the need for a current transformer or complicated waveform synthesis circuitry.

The accuracy and true "square-knee" characteristic of the UC3886 over current limit programming eliminates the need to over-design the power components for operation in an indefinite short circuit.

Accuracy

The typical ±0.5% accuracy of the UC3910 is not corrupted by the UC3886, as the UC3886 uses a very low offset Voltage Amplifier, has very low bias currents, and offsets the bias currents within the IC. The combined system accuracy is ±1%. This high DC accuracy negates the need for trimming the power supply output voltage in manufacturing.

Efficiency

The high current drive of the UC3886 allows the use a high end low R_{DSon} N-channel MOSFET. Full

load efficiencies of 80% can be met with a minimal cost and parts count.

Severe Transient Loading

The UC3886 Average Current Mode Control features allow optimization of both the voltage and current loops. High gain in the current loop can be achieved with Average Current Mode control. The UC3886 features very fast amplifiers for optimal large signal performance. The voltage and Current Amplifiers are internally clamped to reduce their dynamic range, which prevent large overshoot and respond faster to changes in load current. The UC3910 high accuracy allows a tightly regulated DC voltage which allows a wider voltage swing under load transient conditions.

SUMMARY

Power supply requirements for low voltage, high end processors are particularly difficult to meet with regard to tight regulation and fast transient response. The UC3886 contains all the features required to meet these requirements while maintaining high efficiency and a low external parts count. Average current mode control offers excellent regulation and fast transient response, accurate current limiting reduces electrical and thermal overdesign, and high side N-MOSFET drive helps create a simple and high efficiency power circuit.

REFERENCES

[1] Unitrode Application Note U-128, The UC3823A,B and UC3825A,B Enhanced Generation of PWM Controllers, Bill Andreycak

2] Unitrode Application Note U-111, Practical Considerations in Current Mode Power Supplies

[3] Unitrode Application U-133A, UCC 3800/1/2/3/4/5 BiCMOS Current Mode Control ICs, Bill Andreycak

[4] Unitrode Application Note U-140, Average Current Mode Control of Switching Power Supplies, Lloyd Dixon

[5] Unitrode Power Supply Design Seminar SEM-800, Switching Power Supply Control Loop Design, Lloyd Dixon. Reprinted in SEM-900 and SEM-1000.

[6] MOTOROLA Power MOSFET Transistor Data Book, Motorola, Phoenix, Arizona.

[7] HEXFET Power MOSFET Designer's Manual, International Rectifier, El Segundo, California.

[8] Unitrode Application Note U-118, New Driver ICs Optimize High Speed Power MOSFET Switching Characteristics, Bill Andreycak

[9] Unitrode Application Note U-137, Practical Considerations in High Performance MOSFET, IGBT and MCT Gate Drive Circuits, Bill Andreycak

[10] Unitrode Application Note U-158, The UC3910 Combines Programmability, Accuracy and Integrated Functions to Control and Monitor High End Processor Power Supplies, Larry Spaziani

[11] Unitrode Application Note U-157, Fueling the MegaProcessor – A DC/DC Converter Design Review Featuring the UC3886 and UC3910, Larry Spaziani

APPENDIX 1: BUCK REGULATOR BASICS

A schematic of a basic Buck regulator power stage is shown in Figure 1A . Several parasitic elements are included for the reasons described below.

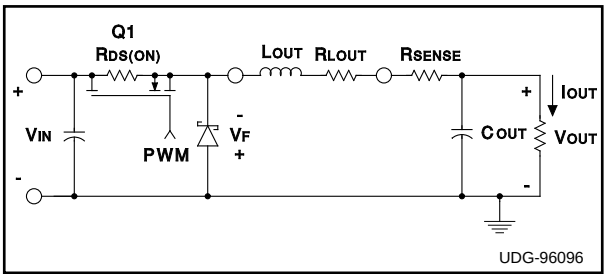

Figure 1A - Buck Regulator Power Stage

The transfer function of a Buck regulator is often simplified as

$$V_{OUT} = V_{IN} - D \qquad \text{Simple Approximation}$$

where D is the duty cycle of the Pulse Width Modulator (PWM).

Parasitic elements such as series resistance and even the diode drop, V_F, are often assumed to be negligible, especially when the output voltage is large compared to these voltage drops, and current is low.

For a low voltage, high current Buck regulator, a more exact transfer function is necessary to insure proper operation.

The basic operation of a Buck regulator with PWM control is this: a PWM controlled rectangular waveform is created by the switch, Q1, and is averaged by the output LC power stage. The inductor must balance volt-seconds during both the ON time and the OFF time in order for this averaging function to occur. Volt-seconds is defined as the product of the voltage across the inductor and the time which that voltage is present.

The equation for the volt-second product across the inductor during the ON and OFF times are given by:

$$VOLT\_SEC\_ON = (V_{IN} - I_{OUT} \bullet (R_{DSON} + R_{LOUT} + R_{SENSE}) - V_{OUT}) \bullet T_{ON}$$

$$VOLT\_SEC\_OFF = (V_{OUT} + I_{OUT} \bullet (R_{LOUT} + R_{SENSE}) + V_F) \bullet T_{OFF}$$

Equating the volt seconds gives

$$(V_{IN} - I_{OUT} \bullet (R_{DSON} + R_{LOUT} + R_{SENSE}) - V_{OUT}) \bullet T_{ON} = (V_{OUT} + I_{OUT} \bullet (RL_{OUT} + R_{SENSE}) + V_F) \bullet T_{OFF}$$

Duty cycle D is defined as T_{ON}/T, where T is the switching period. Therefore, T_{OFF}/T can be defined as 1-D, resulting in

$$\frac{T_{ON}}{T_{OFF}} = \frac{D \bullet T}{(1\text{-}D) \bullet T} =$$

$$\frac{V_{OUT} + [I_{OUT} \bullet (R_{LOUT} + R_{SENSE})] + V_F}{V_{IN} - [I_{OUT} \bullet (R_{DSON} + R_{LOUT} + R_{SENSE})] - V_{OUT}}$$

giving the governing equation for the output voltage

$$V_{OUT} = (D \bullet V_{IN}) - (D \bullet I_{OUT} \bullet R_{DSON}) - [I_{OUT} \bullet (R_{LOUT} + R_{SENSE})] - [V_F \bullet (1 - D)]$$

and the governing equation for duty cycle

$$D = \frac{V_{OUT} + [I_{OUT} \bullet (R_{LOUT} + R_{SENSE})] + V_F}{V_{IN} - (I_{OUT} \bullet R_{DSON}) + V_F}$$

Duty Cycle for Buck Regulator

Example:

V_{IN} = 5.0V

V_{OUT} = 3.1V

R_{LOUT} = 0.010W

R_{SENSE} = 0.010W

R_{DSON} = 0.025W

I_{OUT} = 1A min to 10A max

V_F = 0.4V @ 1A, 0.5V @ 10A

Estimate Duty cycle based on the simple duty cycle approximation:

$$D = \frac{V_{OUT}}{V_{IN}} = \frac{3.1V}{5.0V} = 62\%$$

Calculate Duty cycle based on the complete equation:

$$D = \frac{3.1V + [10A \bullet (0.01W + 0.01W)] + 0.5V}{}$$

= 72.4%@10A

$$D = \frac{3.1V + [1A \bullet (0.01W + 0.01W)] + 0.4V}{5.0V - (110A \bullet 0.025W) + 0.4V}$$

= 65.5%@1A

The results show that simplifying the transfer function can result in a substantial error when low voltages and high currents are considered.

APPENDIX 2: CALCULATING AVERAGE GATE DRIVE CURRENT, I_{GATE}

A MOSFET gate requires a total gate charge, Q_G, which is specified in the manufacturer's data sheet, in order to effectively turn on. Understanding gate drive requirements and dynamics is discussed in detail in U-118 [8] and in U-137 [9]. The MOSFET gate is charged up at turn-on by a peak current waveform, often limited by the driver output impedance as well as series resistance. Over many cycles, the peaks of current can be averaged. This average current must be supplied to the UC3886 from the V_{CC} source.

Figure 2A shows an N-channel MOSFET in a Buck regulator configuration. The input voltage is 5V, and the gate driver is powered from 12V. The effective Gate-to-Source voltage is therefore 7V.

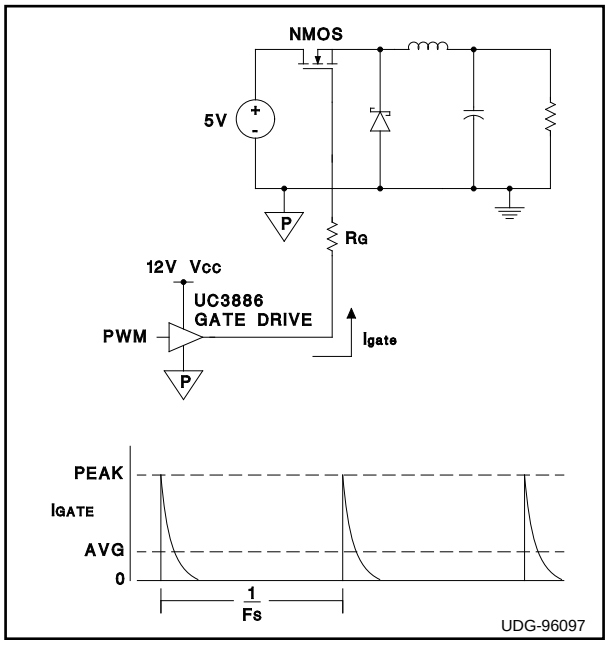

Figure 2A. Calculating Average Gate Current

Figure 2B is a generic example of a manufacturer's "Gate-Source Voltage vs Gate Charge" curve, found in most MOSFET data sheets. The charge required is a direct function of the Gate-to-Source voltage which drives the MOSFET. Using this curve, the required gate charge for the circuit in Figure 2A can be read off of the curve.

Gate charge and current are related by

$$Q_G = I_{GATE} \bullet T_S$$

where I_{GATE} is the AVERAGE gate current and T_S is $1/F_S$ or one switching period.

Average gate current, I_{GATE}, can therefore be calculated by using

$$I_{GATE} = Q_G / T_S = Q_G \bullet F_S.$$

As an example, an IRFZ48 MOSFET requires approximately 50 nanocoulombs total gate charge (Q_G) with 7 volts V_{GS} drive. The average current drawn by the gate at an operating frequency of 200kHz is therefore

$$I_{GATE} = 50nC \bullet 200kHz = 10 \text{ milliamps.}$$

The total current drawn by the UC3886 under these operating conditions, would therefore be

$$I_{CC} = I_{BIAS} + I_{GATE} = 10mA + 10mA$$
$$= 20mA \text{ total.}$$

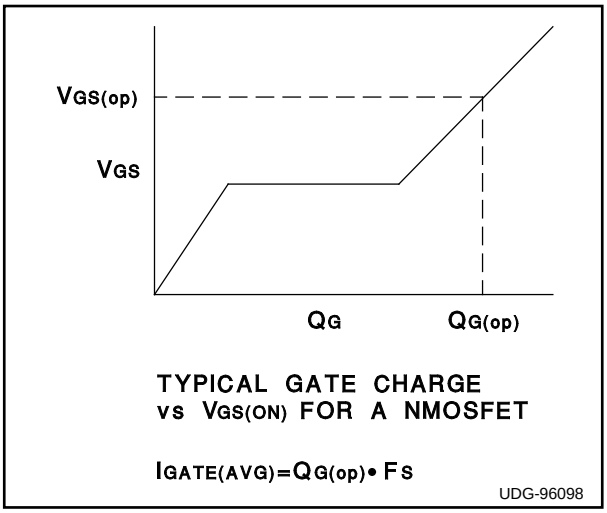

Figure 2B. Using Total Gate Charge to Calculate Gate Current

APPENDIX 3: MANAGING REGULATION AT THE LOAD WITH NON-INTEGRATING GAIN

A model of an Average Current Mode controlled Buck regulator is shown in Figure 3A. The Average Current Mode control loop can be modeled as a simple transconductance amplifier, which converts the Voltage Amplifier's error voltage into the required average output current.

The parasitic resistive and inductive elements shown in the circuit will have the following effects:

- The resistive elements will cause a steady state load regulation error proportional to resistance and load current
- The resistive elements will cause a transient voltage drop proportional to resistance and amplitude of the change in load current
- The inductive elements will cause a transient voltage drop proportional to inductance and the rate of change, di/dt.

Sensitive loads, such as high end Processor ICs, require regulation at the load to be extremely tight under load variations. Load regulation specifica-

tions can consist of a window of voltage regulation which includes variations of steady state load current, load transient conditions, voltage ripple and DC regulation tolerances.

The allowed transient voltage deviation, when considering low voltage processors with very fast transients rates, can be extremely difficult to meet, and may require an excessive amount of output capacitance in order to keep the total capacitor's ESR and ESL low enough to meet the regulation requirements. Excess capacitance is bulky and expensive.

Managing the regulation at the load can be summarized by the following goals and methods to meet the goals.

Goals

1. Meet ±5% regulation at the load under all operating conditions
2. Minimize the amount of output capacitance required at the power supply output in order to minimize cost and size

Methods

1. Use parallel, low impedance pins at the power supply connector.
2. Use power and ground planes from the power supply to the load.
3. Maximize local decoupling at the load.
4. Minimize ripple to maximize use of the regulation window.
5. Compensate for the I • R voltage drop to the load with positive DC offset at the power supply output.
6. Maximize allowable transient voltage swing by providing positive DC offset at the power supply output when operating at the minimum load, and providing negative DC offset at the power supply output when operating at the maximum load. This can be accomplished by using Non integrating gain (resistive, not capacitive feed back) about the Voltage Amplifier.

Methods 1 through 4 consist of good electronic layout and filtering practices. Methods 5 and 6 are steps which can be taken at the power supply, and are discussed below.

Figure 3B illustrates the output voltage effects resulting from load transients when integrating and non-integrating feedback is utilized as well as the effects of a DC offset voltage.

Integrating gain utilizes a DC blocking capacitor in the feedback, and therefore results in a very high

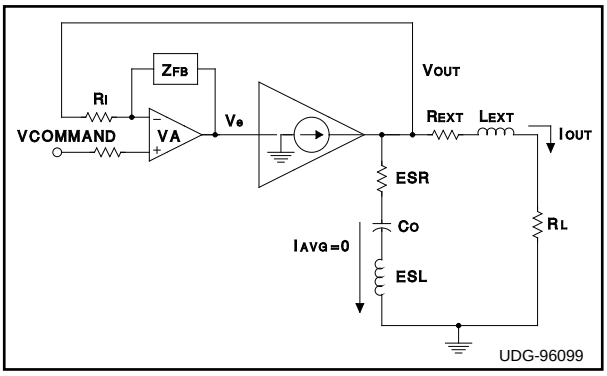

Figure 3A. Average Current Mode Controlled Regulator Output Model

DC gain. The result is excellent load regulation, where the output voltage is nominally equal to the command voltage. This is typical of most power supplies.

Non-integrating gain utilizes a resistive feedback path instead of capacitive. The result is that the output voltage will decrease as the load current increases. This provides an INTENTIONAL negative load regulation characteristic.

The use of the DC offset, achieved simply by the voltage divider formed by R_I and R_D of Figure 3B, centers the output voltage at nominal load.

These points are best shown by an example.

EXAMPLE

Buck regulator using UC3886/UC3910 Chip Pair

V_{OUT} = 2.4V to 3.4V.

Regulation window = ±5% including load, line, ripple and transient conditions.

Ripple = ±1%

DC Regulation Tolerance plus Line Regulation = ±1%

I • R Voltage Drop from power supply to load = -1% at Imax

Imin = 0.5A = Minimum normal operating current

Imax = 10A = Maximum normal operating current

I_Limit = 12A = Short circuit current limit

Goal: Determine and set V_{OUT} vs I_{OUT} such that the ±5% Regulation requirement is met with maximum allowed transient voltage swings (minimum output capacitance).

Step 1: Establish a regulation goal.

The specified window is ±5%. V_{RIPPLE} and DC Error, which are each ±1%,

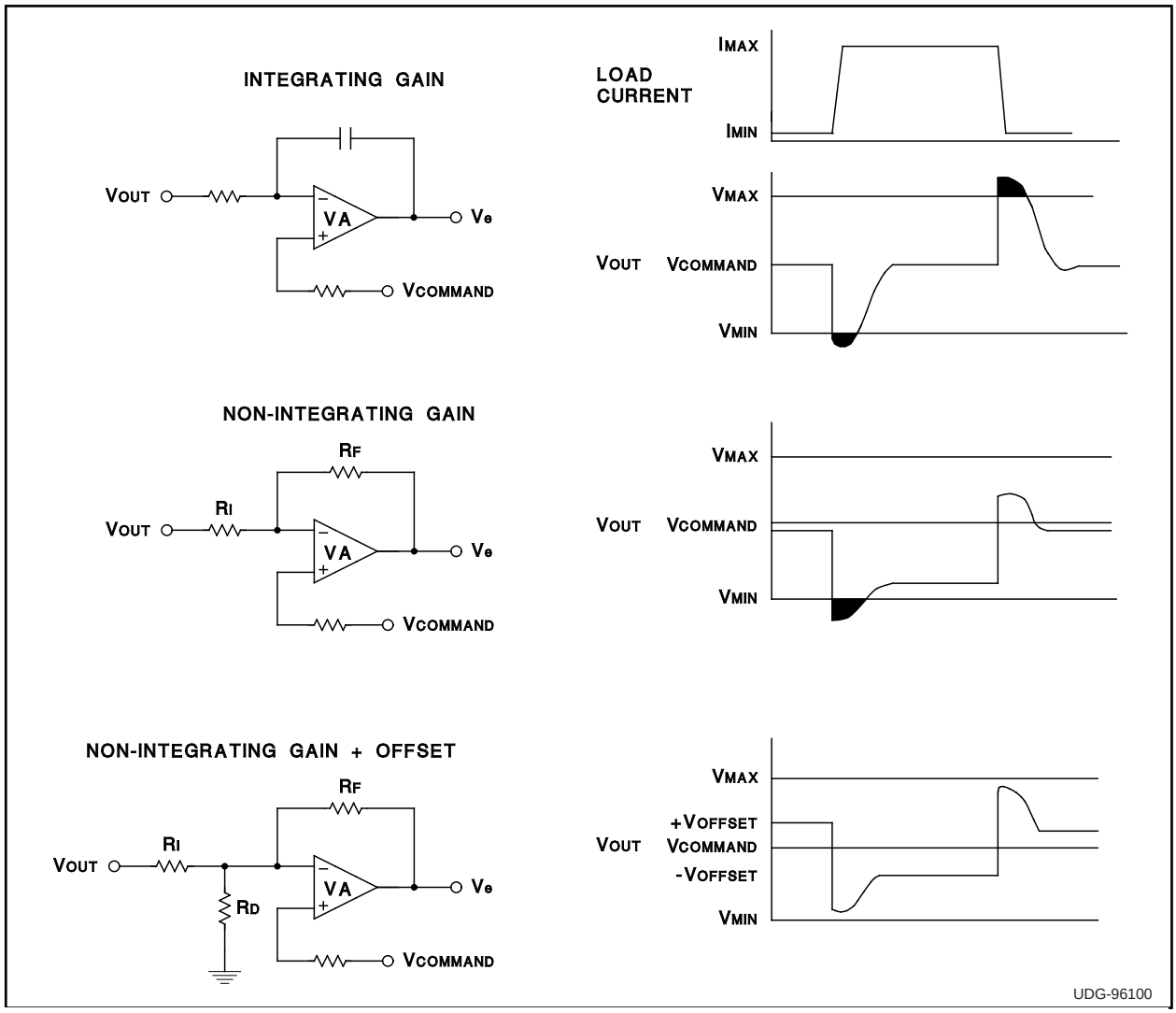

Figure 3B. Integrating vs Non-Integrating Gain in the Voltage Error Amplifier of the UC3886

reserve ±2% of the specified window. This leaves ±3% of the window for load regulation.

Figure 3C illustrates the regulation window.

Based on the regulation of integrating gain, a load step from Imin to Imax may only cause a -3% voltage excursion and still insure that the ±5% window requirement is met. The load regulation set as a goal will double the allowed voltage excursion from -3% to -6%.

Step 2: Determine the voltage-to-current gain of the closed loop Average Current Mode circuit.

The UC3886 error voltage, COMP, swings from Vcommand at 0.0 amperes load current, to $V_{COMMAND}$ +1.0V at the short circuit current limit point, I_Limit, set by the Current Sense Amplifier gain. The voltage-to-current gain is therefore equal to

$$V\_to\_I\_Gain = \frac{I\_Limit}{DVe} = \frac{12\ A}{1.0\ V} = 12$$

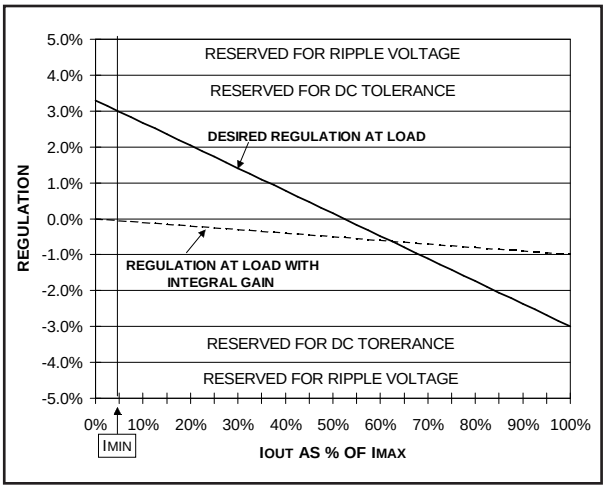

Figure 3C. Load Regulation for Example Circuit

Step 3: Determine the swing in the UC3886 error voltage, COMP, at Imax.

$$DVe = \frac{Imax}{I\_Limit} \bullet 1.0 = \frac{10.0\ A}{12\ A} \bullet 1.0$$

$$= 0.833\ Volts$$

From the desired load regulation curve, determine the swing in output voltage associated with the change from 0 Amps (Not Imin in this case) to Imax. Subtract the I • R drop intrinsic to the circuit.

The desired regulation swing is -6.3% - (-1.0%) = -5.3% from 0A to Imax. At the lowest operating output voltage, this is equivalent to:

$$DV_{OUT} = 2.4V \bullet 5.3\% = 0.127\ Volts$$

Step 4: Determine the gain around the Voltage Amplifier to achieve the desired voltage swing over the operating load range.

$$DVout = \frac{DVe}{Gain} = \frac{DVe}{R_F/R_I}$$

and therefore $R_F/R_I = \frac{0.833V}{0.127V} = 6.56$

Where R_F is the feedback resistor and R_I is the input resistor, as in Figure 3B. Let R_F = 20.0kW, then R_I = 3.09kW and the gain about the Voltage Amplifier = 6.47.

Step 5: Determine the DC offset required from the Resistive Divider and calculate the value of R_D.

The resistive divider must offset the output voltage by the desired offset at 0.0 Amps of +3.3%.

Using a voltage divider resistor, R_D with R_I, as shown in Figure 3B:

$$\frac{R_D}{R_I + R_D} = 1 - 0.033 \text{ so}$$

$$R_D = \frac{R_I \bullet (1-0.033)}{0.033} = 90.9kW$$

Figure 3D illustrates the resulting load regulation at the output of the power supply and at the load.

Step 6: Determine the effects of a variable output voltage

The DC offset fixed by the voltage divider of R_I and R_D is setting an offset percentage, which is constant at 3.3%.

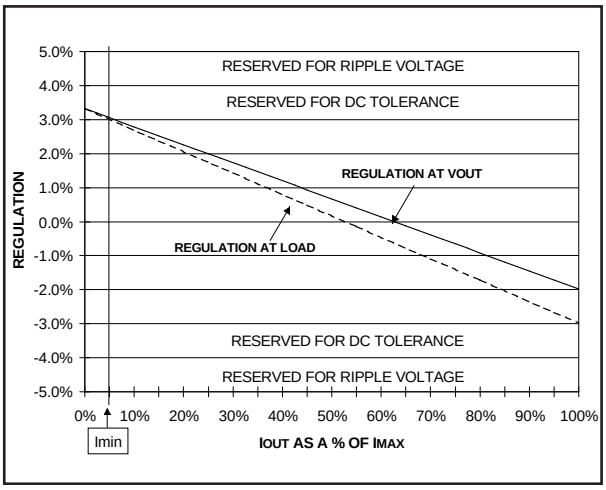

Figure 3D. Load Regulation for Example Circuit -2.4V Output

Therefore, at 0.0A all output voltages will start at +3.3% offset.

The gain of the Voltage Amplifier, set by R_F and R_I, is also fixed, and will therefore have a smaller effect at output voltages larger then 2.4V. At 3.4V, the change in output voltage is fixed at -0.127 Volts, which is only -3.74% of the nominal output. The higher voltages will therefore operate within a narrower voltage regulation window than 2.4V and the voltage regulation requirements will be met.

APPENDIX 4: DIFFERENTIAL AMPLIFIER EQUATIONS

The amplifier shown in Figure 4A is configured as a differential amplifier, with a DC bias. The output voltage of this configuration is given by

$$V_{OUT} = V_{BIAS} + (V1 - V2) \bullet \frac{R2}{R1}$$

This result can be derived from the principal of superposition, by adding the portion of the output voltage due to each input voltage, V1, V2 and V_{BIAS}.

V1 term: Set V_{BIAS} and V2 to GND, find V_{OUT}:

The voltage at the non-inverting input to the amplifier V(+) is derived from the voltage divider of R2 and R1, and is then multiplied by the non-inverting op-amp non-inverting gain formula.

$$V(+) = V1 \bullet \left(\frac{R2}{R1+R2}\right)$$

$$V_{OUTV1} = V(+) \bullet \left(1 + \frac{R2}{R1}\right)$$

$$= V1 \bullet \left(\frac{R2}{R1+R2}\right) \bullet \left(1 + \frac{R2}{R1}\right)$$

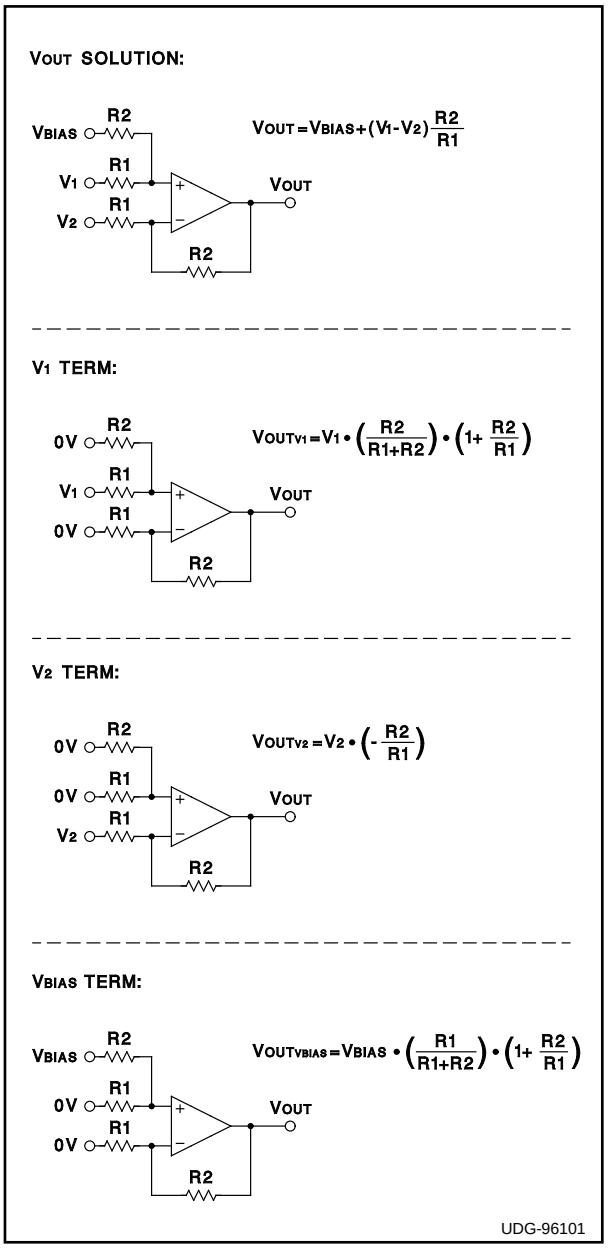

Figure 4A. Differential Amplifier Configuration with DC Bias

V2 term: Set V_{BIAS} and V1 to GND, find V_{OUT}:

The voltage at the non-inverting input to the amplifier is 0 volts. The configuration is therefore a standard inverting op-amp configuration which gives

$$V_{OUTV2} = V2 \bullet \left(-\frac{R2}{R1}\right)$$

V_{BIAS} term: Set V1 and V2 to GND, find V_{OUT}:

The voltage at the non-inverting input to the amplifier is derived from the voltage divider of R1 and R2, and is then multiplied by the non-inverting op-amp non-inverting gain formula.

$$V(+) = V_{BIAS} \bullet \left(\frac{R1}{R1+R2}\right)$$

$$V_{OUTVBIAS} = V(+) \bullet \left(1 + \frac{R2}{R1}\right)$$

$$= V_{BIAS} \bullet \left(\frac{R1}{R1+R2}\right) \bullet \left(1 + \frac{R2}{R1}\right)$$

when factored gives

$$V_{OUTVBIAS} = V_{BIAS}$$

V_{OUT} Solution: Sum the 3 terms together

$$V_{OUT} = V1 \bullet \left(\frac{R2}{R1+R2}\right) \bullet \left(1 + \frac{R2}{R1}\right)$$

$$+ V2 \bullet \left(-\frac{R2}{R1}\right) + V_{BIAS}$$

which yields

$$V_{OUT} = V_{BIAS} + (V1 - V2) \bullet \frac{R2}{R1}$$

The DC Bias is the value of V_{BIAS}, and the gain of the differential amplifier which multiplies the difference voltage (V1 - V2) is given by

$$\text{Gain} = \frac{R2}{R1}$$

APPENDIX 5: PROGRAMMING THE SHORT CIRCUIT LIMIT

From the short circuit current equation

$$I_{SC} = \frac{1.0 \text{ volt}}{R_{SENSE} \bullet G_{CSA}}$$

it can be seen that the product of the sense resistor and the gain of the Current Sense Amplifier must be

$$R_{SENSE} \bullet G_{CSA} = \frac{1.0 \text{ Volt}}{I_{SC}}$$

The value of G_{CSA} is bounded to

$$G_{CSA\_MIN} = 5.0 \text{ and } G_{CSA\_MAX} = \frac{2.5MHz}{F_{SWITCH}}$$

which in turn, bounds the value of R_{SENSE}, since the product is a constant.

Several considerations must be used to select R_{SENSE}:

- Type - 2 Wire vs 4 Wire: With very low value sense resistors, as the UC3886 allows, the resistance of the solder joint becomes a major contributor to resistance. A 4 wire Kelvin connection removes the error due to the solder joint. A 2 wire is more cost effective. A compromise may be in using a surface mount 2 wire resistor and splitting the pads to simulate a 4 wire connection. Beware that paralleling 4 wire

resistors for reduced power dissipation can result in an imbalance between the resistors.

- Value - Minimum and Maximum possible values: The upper value is limited by the minimum G_{CSA} value, and the lower value by the maximum G_{CSA} value. Higher values dissipate more power. Lower values typically have a higher temperature coefficient, resulting in less accuracy over temperature and have a higher cost factor.
- Efficiency and Power Dissipation: The lower the value of R_{SENSE}, the less power dissipation and the higher the regulator's efficiency. Power dissipation must be considered under both normal maximum operating current, Imax, as well as under short circuit conditions, I_{SC}.
- Operating Voltages and Duty Cycle: Given a low input voltage and an output voltage close to V_{IN}, such as 3.3V input, 2.9V output, the operating duty cycle can be quite high. A large voltage drop across R_{SENSE} may be unacceptable.
- Self-Inductance: A low inductance type of resistor should be used. Inductance of the resistor will result in an inductive "step" voltage superimposed on the ramp voltage. The step voltage will not contribute to error as the average current measurement is not effected, but may contribute to instability due to the very high slope of the inductive step. Refer to Unitrode Application Note U-140 [4] regarding slope limitations in Average Current Mode Control.

The following example illustrates the selection process in choosing R_{SENSE} and in setting the value of G_{CSA}.

F_{SWITCH}: 200kHz

Imax: 10.0A

I_{RIPPLE}: 1.0Ap-p

R_{LOUT} 0.01W

V_F 0.5V @ 12A

V_{IN} 5.0V

$R_{DS(on)}$ 0.025W

Step 1: Find the bounds of the Current Sense Amplifier gain G_{CSA}.

Minimum gain = 5.0 By specification

$$\text{Maximum gain} = \frac{2.5\text{MHz}}{200\text{kHz}} = 12.5$$

Step 2: Choose the short circuit limit. This limit should insure that tolerances and ripple current do not inadvertently trip the over current threshold.

Figure 5A illustrates the limitations on the sense resistor based on the bounds of the gain. Choosing a value of Isc as low as possible will limit the power dissipation in the sense resistor.

Select I_{SC} = 12.0 Amps.

Step 3: Choose a value of R_{SENSE}

From Figure 5A, a 12.0A I_{SC} implies that Rsense must lie between 0.007W and 0.017W. Choose 0.010W as the lowest standard value.

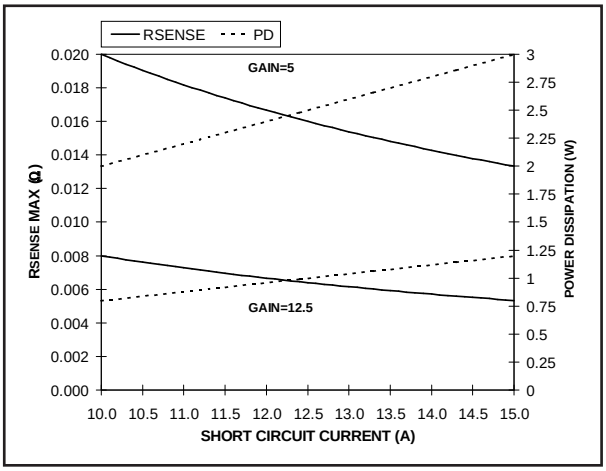

Figure 5A. R_{SENSE} and Power Dissipation Boundaries

Step 4: Program the gain of the Current Sense Amplifier.

$$G_{CSA} = \frac{1.0\text{ Volt}}{I_{SC} \bullet R_{SENSE}}$$

$$= \frac{1.0\text{ Volt}}{12.0\text{A} \bullet 0.01\text{W}} = 8.33$$

Choose large enough resistors so as not to load down the output of the Current Sense Amplifier. Refer to Figure 14 of this application note to configure the Current Sense Amplifier.

Select R2 = 36.5kW

$$R1 = \frac{36.5\text{kW}}{8.33} = 4.42\text{kW}$$ (closest 1% value)

$$G_{CSA} = \frac{36.5}{4.42} = 8.25$$

Step 5: Solve for the minimum AVERAGE short circuit current limit.

The tolerance of the UC3886 current limit clamping mechanism is 1.0V ±0.05V.

Assume R_{SENSE} and G_{CSA} each have a tolerance of ±2% over temperature and life. 1/2 of I_{RIPPLE} will add to the AVERAGE current value of I_{SC}, and should not cause the UC3886 to clamp into over current.

Then

$$I_{SC(min)} + \frac{I_{RIP}}{2} = \frac{0.95\ Volt}{R_{SENSE} \bullet 1.02 \bullet G_{CSA} \bullet 1.02}$$

which gives

$$I_{SC(min)} = \frac{0.95\ Volt}{0.010\Omega \bullet 1.02 \bullet 8.25 \bullet 1.02} - \frac{1.0A}{2} = 10.57\ Amperes$$

which is above the maximum operating current of 10.0 amperes

Step 6: Calculate the power dissipation in R_{SENSE} during normal and short circuit conditions.

Normal: $Pd = Imax^2 \bullet R_{SENSE}$

$= 10^2 \bullet 0.010\Omega = 1.0$ Watt

Short Circuit: $Pd = I_{SC}^2 \bullet R_{SENSE}$

$= 12^2 \bullet 0.010\Omega = 1.44$ Watt

Calculating the Short Circuit Duty Cycle

During a short circuit condition in a Buck regulator, the duty cycle becomes small and the free-wheeling diode conducts current for most of each switching cycle. The free-wheeling diode's average current is almost equivalent to the short circuit current in this condition, resulting in much higher power dissipation.

To calculate the power dissipated in the diode, the short circuit duty cycle, D_{SC}, must be calculated.

The governing equation of the Buck regulator is derived in Appendix 1, where the output voltage is given by

$$V_{OUT} = D \bullet (V_{IN} - I_{OUT} \bullet (R_{DSon}) - [I_{OUT} \bullet (R_{LOUT} + R_{SENSE})] - [V_F \bullet (1-D)]$$

where D is the operating duty cycle. Under a true (0.0Ω) short circuit condition, the output voltage is 0.0 volts and the operating duty cycle will be D_{SC}. Using 0.0V in the formula above and solving for I_{SC} and D_{SC} gives

$$I_{SC} = \frac{D_{SC} \bullet (V_{IN} + V_F) - V_F}{D_{SC} \bullet R_{DSon} + R_{LOUT} + R_{SENSE}}$$

$$\text{and } D_{SC} = \frac{I_{SC} \bullet (R_{LOUT} + R_{SENSE}) + V_F}{V_{IN} - I_{SC} \bullet R_{DSon} + V_F}$$

Continuing from the above example, the short circuit duty cycle is

$$Dsc = \frac{12A \bullet (0.01\Omega + 0.01\Omega) + 0.5V}{5.0V - 12A \bullet 0.025\Omega + 0.5V} = 12\%$$

The resulting diode average current is therefore

I_{DIODE} = (100%-12%) • 12A = 10.56 Amperes.

The output inductor, $L_{OUT,}$ must be designed not to saturate at the short circuit current. Should L_{OUT} saturate, excessive current can result which is only limited only by the parasitic resistances, which can result in reliability or safety problems.

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. 603-424-2410 • FAX 603-424-3460